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65	+1V2_SFROC
66	+VPP
67	+VDDQ
68	+5V & +3.3V
69	+VCCIO
70	+VCCSA
71	+VT
72	+VCORE +VCCGT CONTROLLER
73	+VCORE PHASE 1 & 2
74	+VCCOE PHASE 3
75	+VCCGT PHASE 1 & 2
76	PWR CHANGLIST

# Intel Greenlow Platform

## Skylake CPU / Sunrise PCH

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BOM Definition	
I	Installed
NI	Not Installed
CCL	Critical Components List
PROTO	Not For Production Part
MP	Production Part ONLY

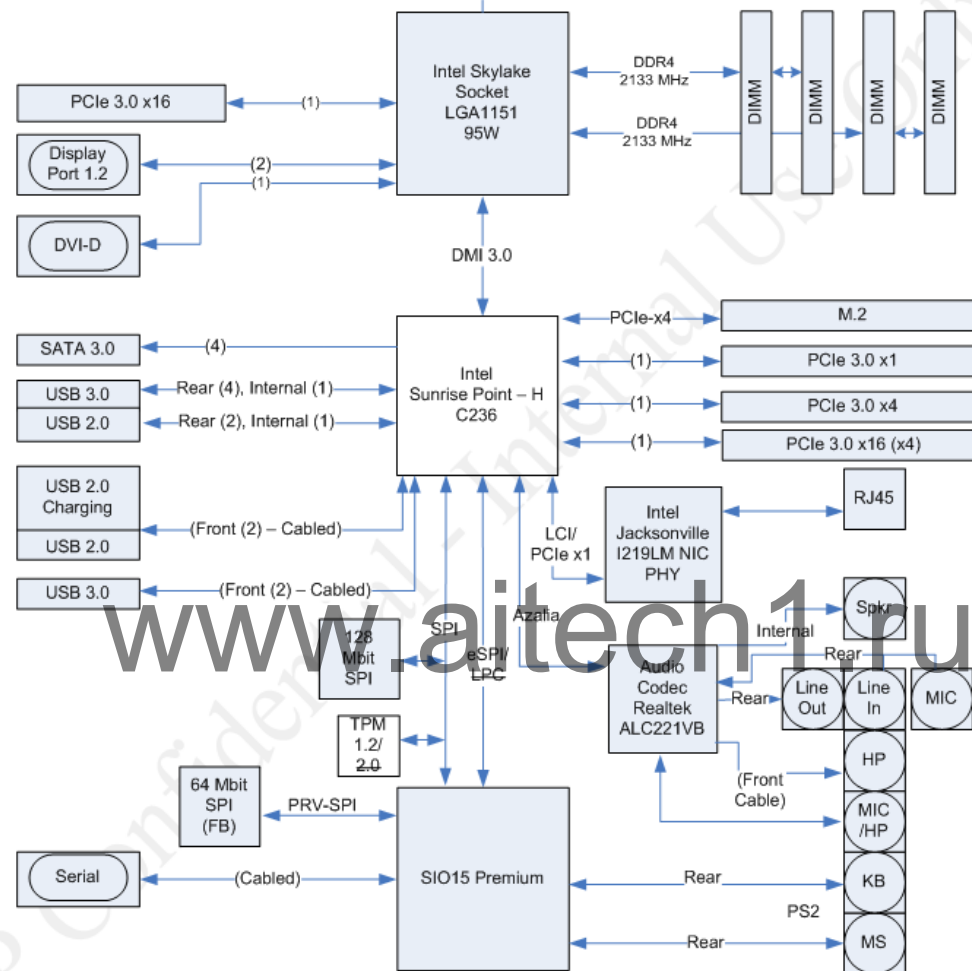
PCA P/N	795000-001
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PCB AND SILKSCREEN COLOR		
Program Phase	Color of PCB	Silkscreen
EVT1	RED	YELLOW
EVT2	RED	WHITE
EVT3	RED	WHITE
DVT1	GREEN	YELLOW
DVT2+, Pre-PVT	GREEN	WHITE
PVT1	DARK BLUE	YELLOW
PVT2+	DARK BLUE	WHITE
SP/MP/B / PRODUCTION	DARK BLUE	WHITE

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Title
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### BLOCK DIAGRAM

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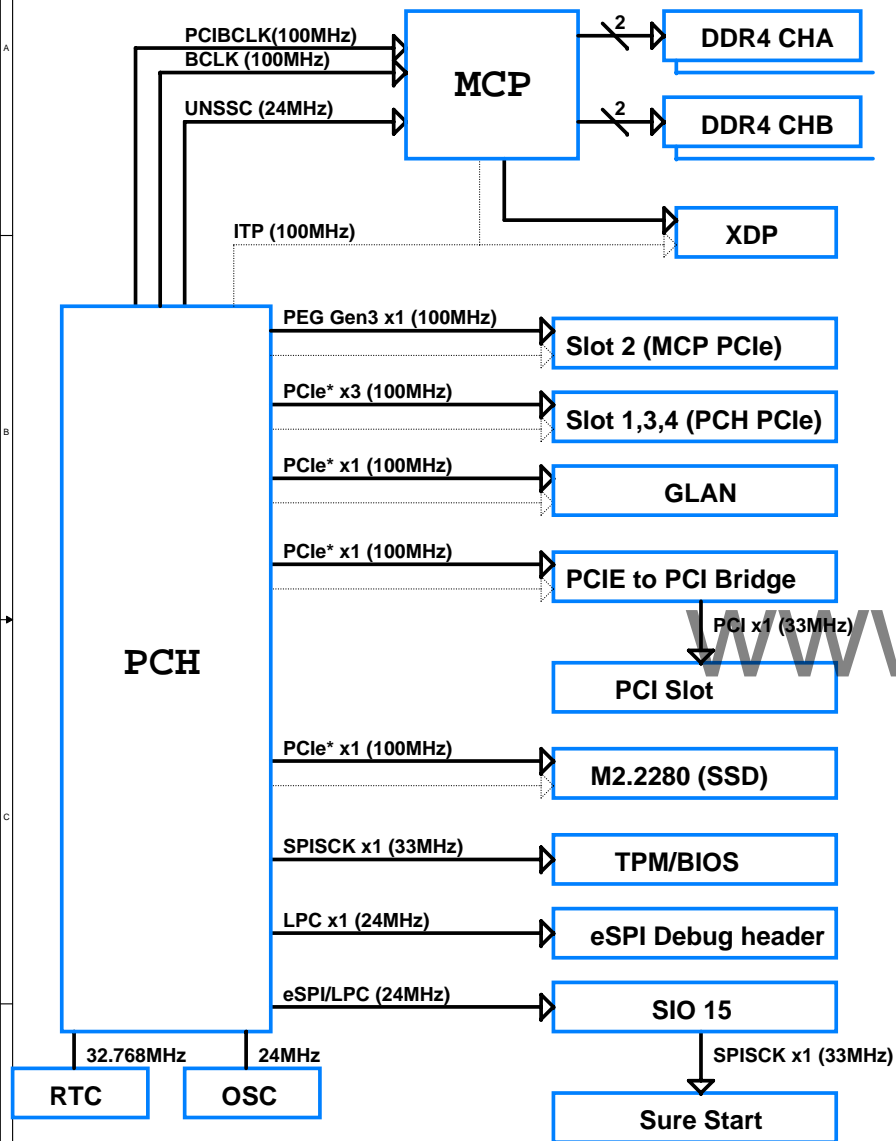
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Rev  
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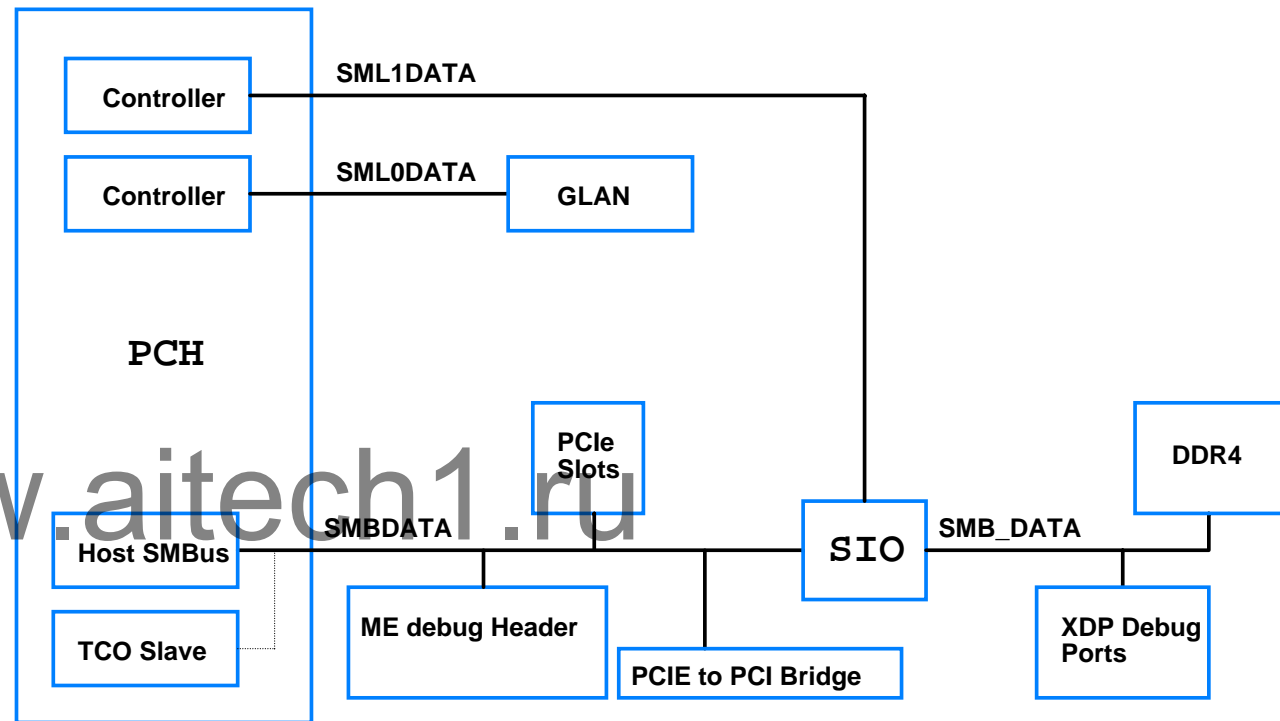
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16:17:08 (UTC/GMT) Sheet 2 of 76

# Clock Diagram



# SMBus Block Diagram



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**POWER SUPPLY**  
+12V\_CPU  
+12V\_MAIN  
+12V\_AUX  
-12V

+12V\_CPU  
+12V\_DAUL  
+12V\_DAUL\_CPU

**CPU Core Switcher**  
+VCCIA  
3-phase Switching  
70A (Imax=79A)  
SVID=0.55~1.15V  
  
+VCCGT  
2-phase Switching  
37A (Imax=51A)  
SVID=0.55~1.15V

+VCCIA (0.55~1.5V)  
  
+VCCGT (0.55~1.5V)

**VCC\_DDR Switcher**  
12A

+1.2V\_VDDQ

**+VTT LDO**  
1.1A

+VTT

**VPP\_2.5V Switcher**  
2.24A

+2.5V\_VPP

**+1.0V\_AUX**  
10.66A

+1.0V\_AUX

**5V & 3.3V Switcher**  
  
+5V  
20A  
  
+3.3V  
20A

+5V\_AUX/+5V\_MAIN/+5V\_DUAL  
  
+3.3V\_AUX/+3.3V\_MAIN

**VBAT 3.0**  
VCCRTC

BATT1

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+VCCIA  
Imax=79A  
+VCCGT  
Imax=51A  
+VCCSA  
Imax=11.1A  
+VCCIO  
Imax=5.5A  
+VCCSFR  
Imax=0.11A

**SKL (95W TDP)**  
  
10.66A  
0.4A  
0.203A 0.6699W  
<1mA <3mW

+1.0V\_AUX  
P1V8\_P3V3\_PCH\_GPPA  
+3.3V\_AUX  
+3V\_BATT

**LPT (5.5W TDP)**  
  
10.66A  
0.4A  
0.203A 0.6699W  
<1mA <3mW

+VTT  
+VDDQ

**DDR4 DIMM x4**  
  
1A 0.6W  
12A 14.4W

+3.3V  
+3.3V\_AUX  
+3V\_BATT

**SUPER I/O**  
  
15mA 49.5mW  
20mA 66mW  
1uA 3.3uW

+5V\_AUDIO  
+3.3V\_AUX

**AUDIO**  
  
33mA  
33mA

+3.3V\_Main

**SPI EEPROM**  
30mA 0.1W

+5V\_MAIN

**PARALLEL PORT**  
15mA 75mW

+12V  
+3.3V\_AUX

**SERIAL PORT**  
  
1mA 12mW  
50uA 165uW

+5V\_DUAL

**PS2 KB/M**  
50mA 250mW

+12V

**FAN**  
200mA 2.4W

+3.3V\_LAN

**LAN**  
0.218A 0.7194W

+3.3V\_AUX  
+3.3V\_MAIN  
+12V

**PCIe SLOT x4**  
  
0.375A 1.2375W  
9A 29.7W  
9.7A 116.4W

+5V\_DUAL

**USB PORT x14**  
**3.0 X5 2.0 X9**  
8A 40W

+12V  
+5V\_MAIN

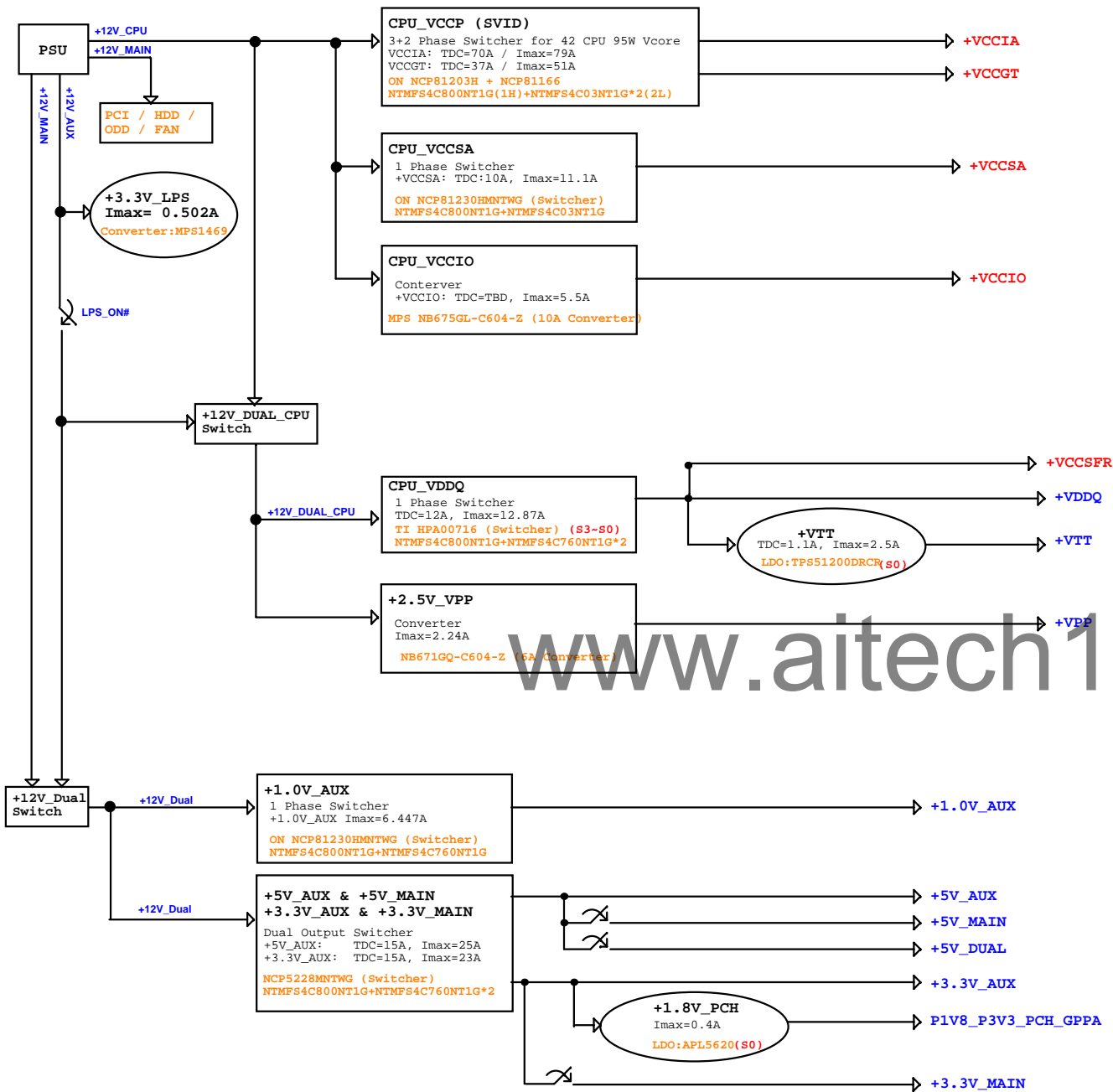
**HARD DRIVER**  
  
0.35A 4.2W  
0.72A 3.6W

+12V  
+5V\_MAIN

**CD ROM**  
  
1.5A 18W  
1.5A 7.5W

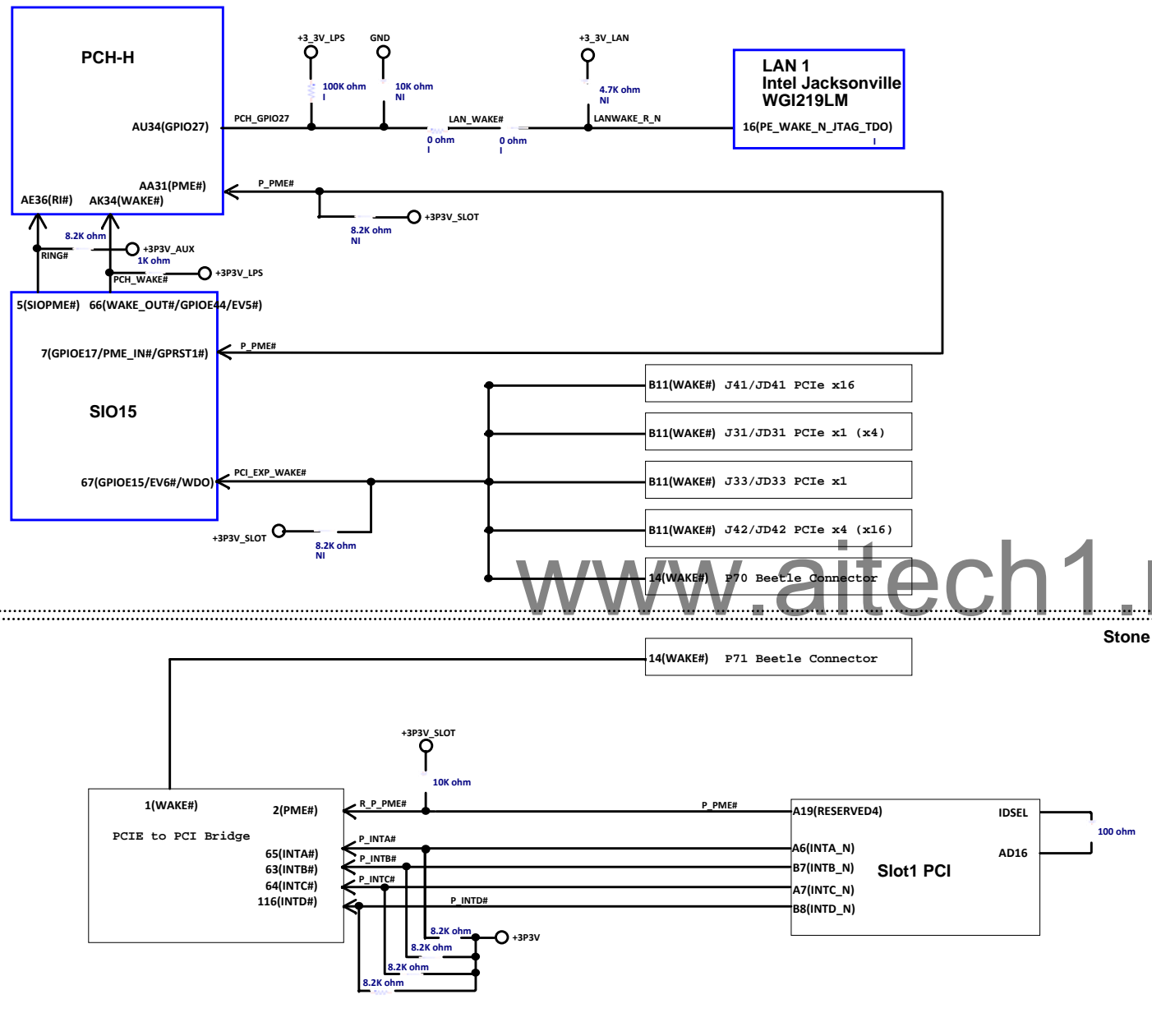
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Size Custom	Document Number <b>Skylake_Ataya1</b>		Rev <b>B</b>
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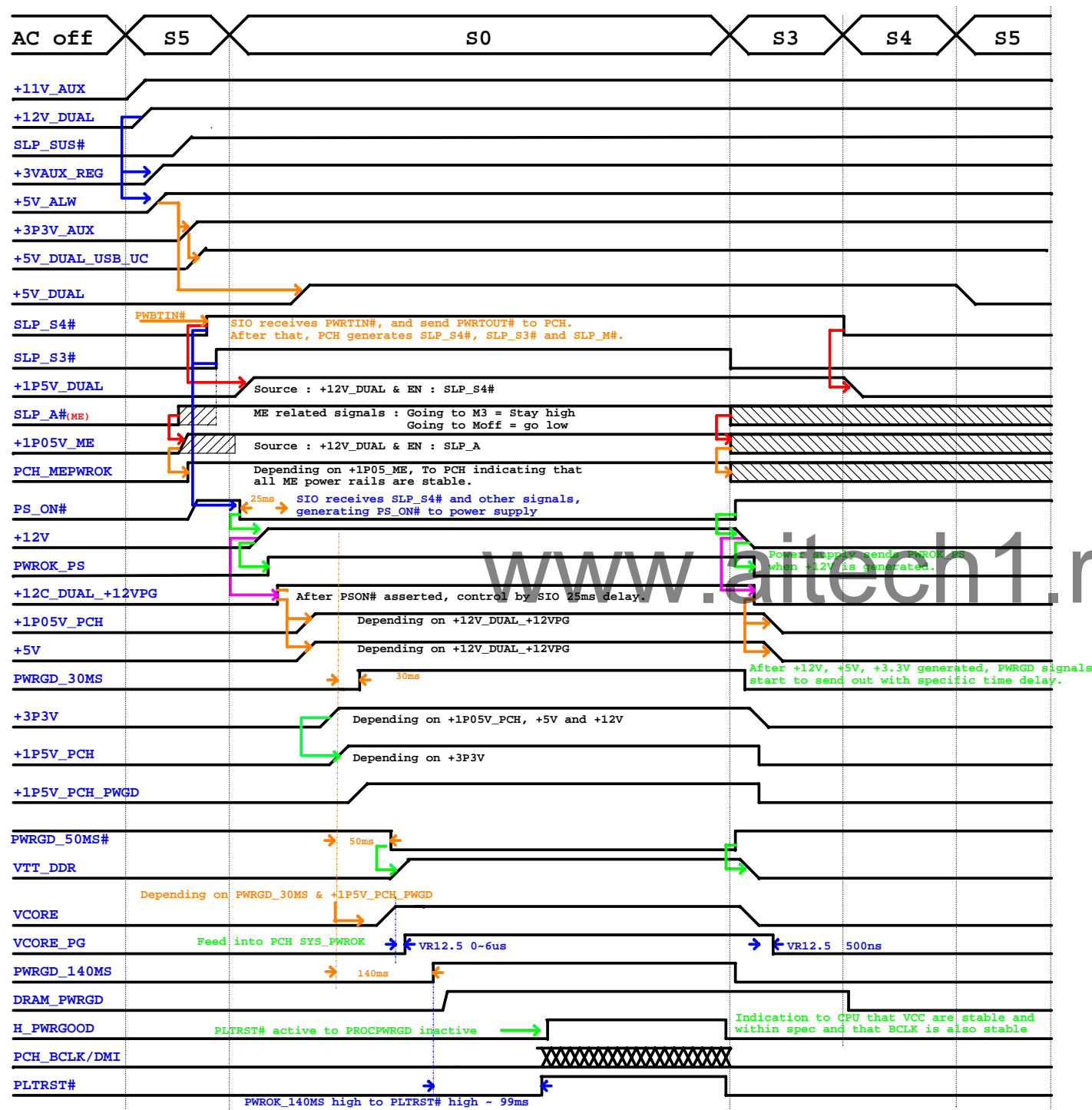
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## Interrupt & PME diagram



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# POWER SEQUENCE DIAGRAM



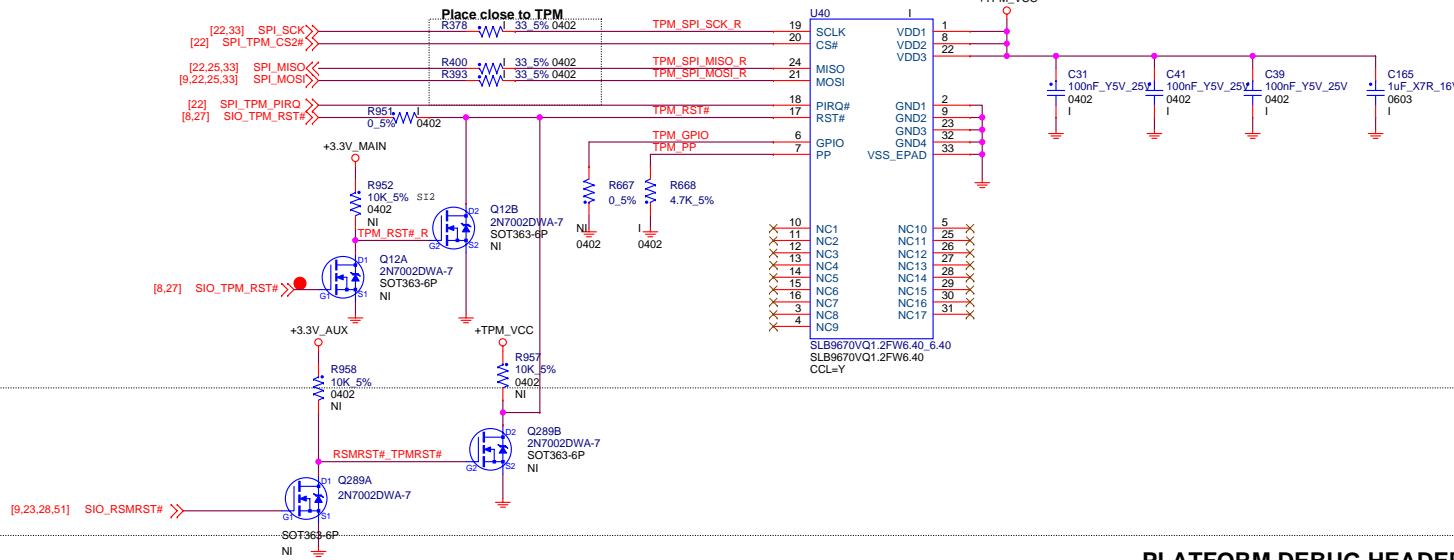
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# TPM

For SLB9670 TPM SPI signal

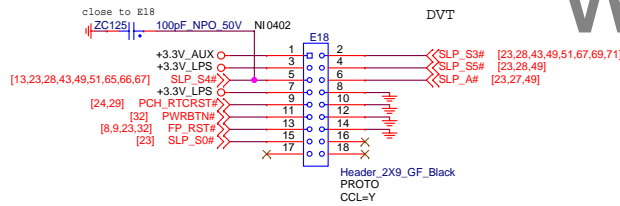
+3.3V\_AUX  
R58  
SHORT-PAD-15  
D603\_15MII

## ME DEBUG HEADER

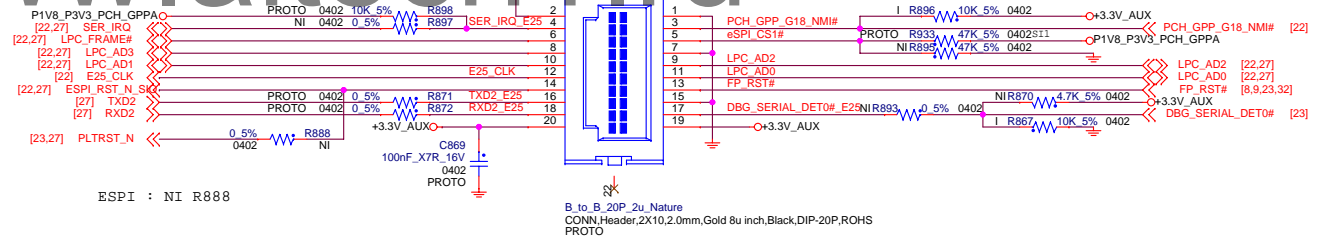


## PLATFORM DEBUG HEADER

### METS/APS TEST HEADER

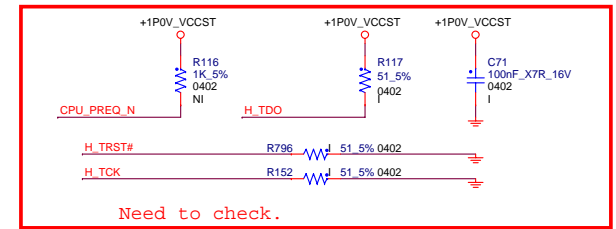
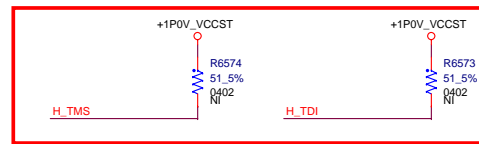


LPC: Install R897, NI R898  
ESPI: NI R897, Install R898

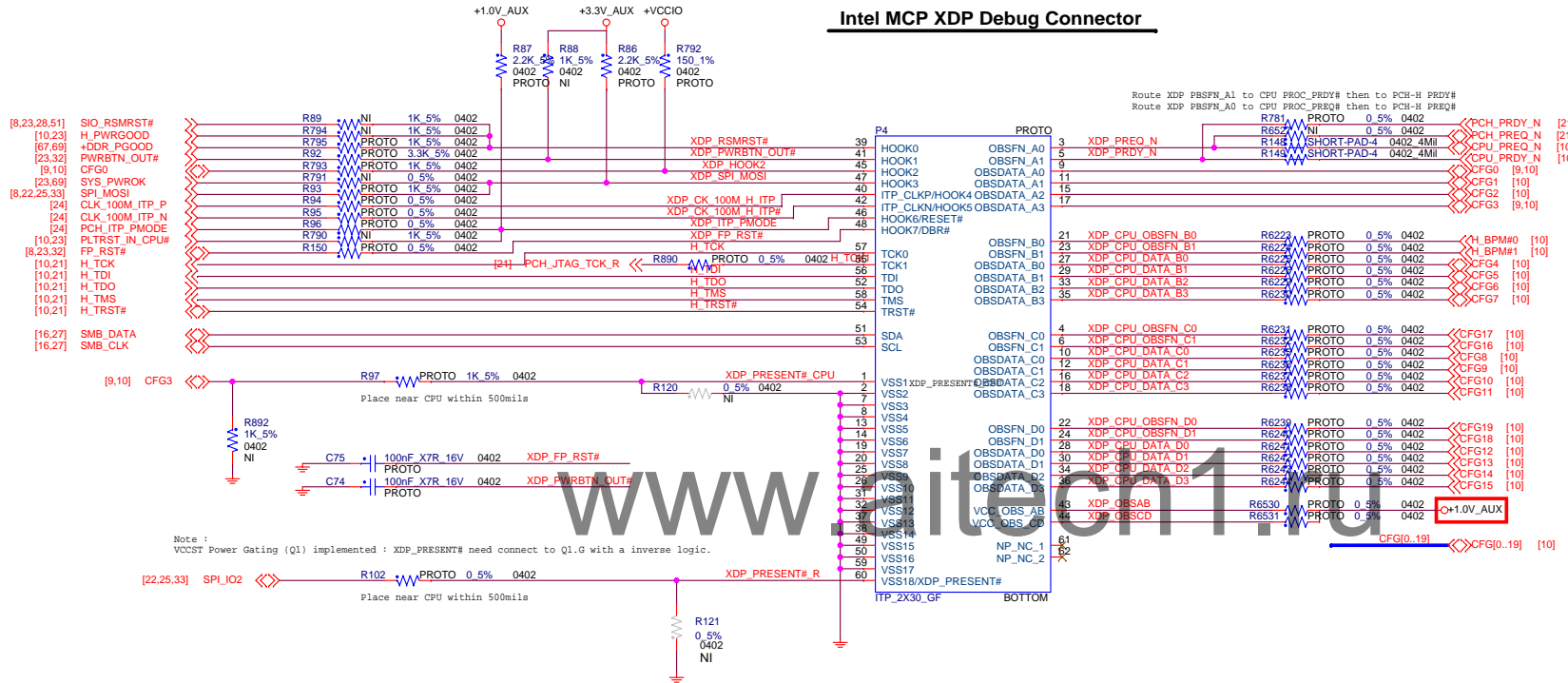


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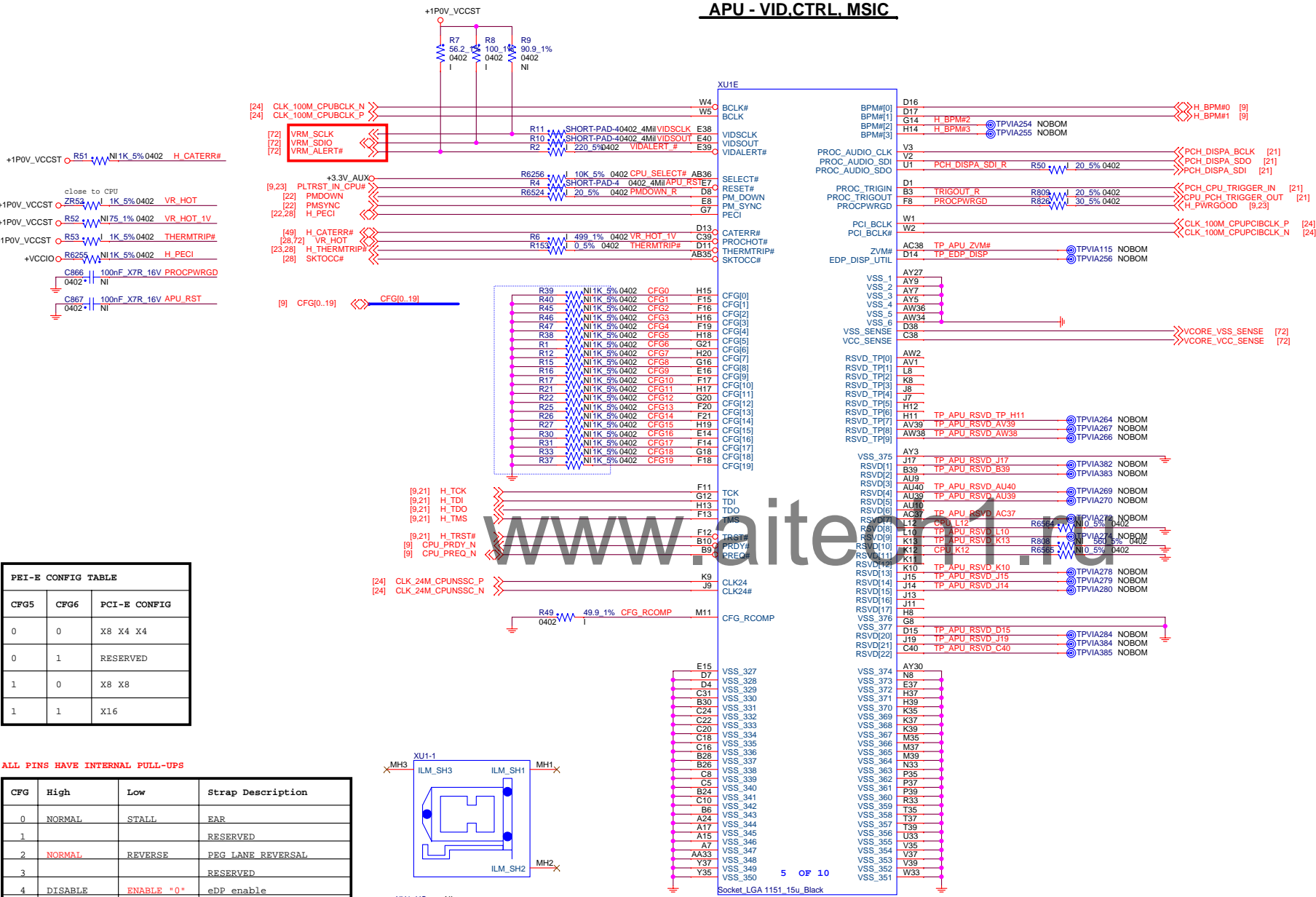


# Intel MCP XDP Debug Connector



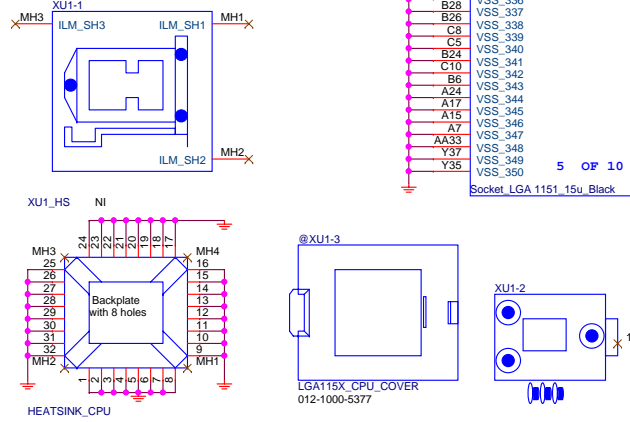
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# APU - VID.CTRL. MSIC



PEI-E CONFIG TABLE			
CFG5	CFG6	PCI-E CONFIG	
0	0	X8 X4 X4	
0	1	RESERVED	
1	0	X8 X8	
1	1	X16	

ALL PINS HAVE INTERNAL PULL-UPS			
CFG	High	Low	Strap Description
0	NORMAL	STALL	EAR
1			RESERVED
2	NORMAL	REVERSE	PEG LANE REVERSAL
3			RESERVED
4	DISABLE	ENABLE "0"	eDP enable
5	DISABLE "1"	DISABLE "1"	PEG0CFGSEL[0] x16
6	DISABLE "1"	DISABLE "1"	PEG0CFGSEL[1] x16
7	RESET N	BIOS REQ	PEG DEFER TRAINING
8-19			RESERVED



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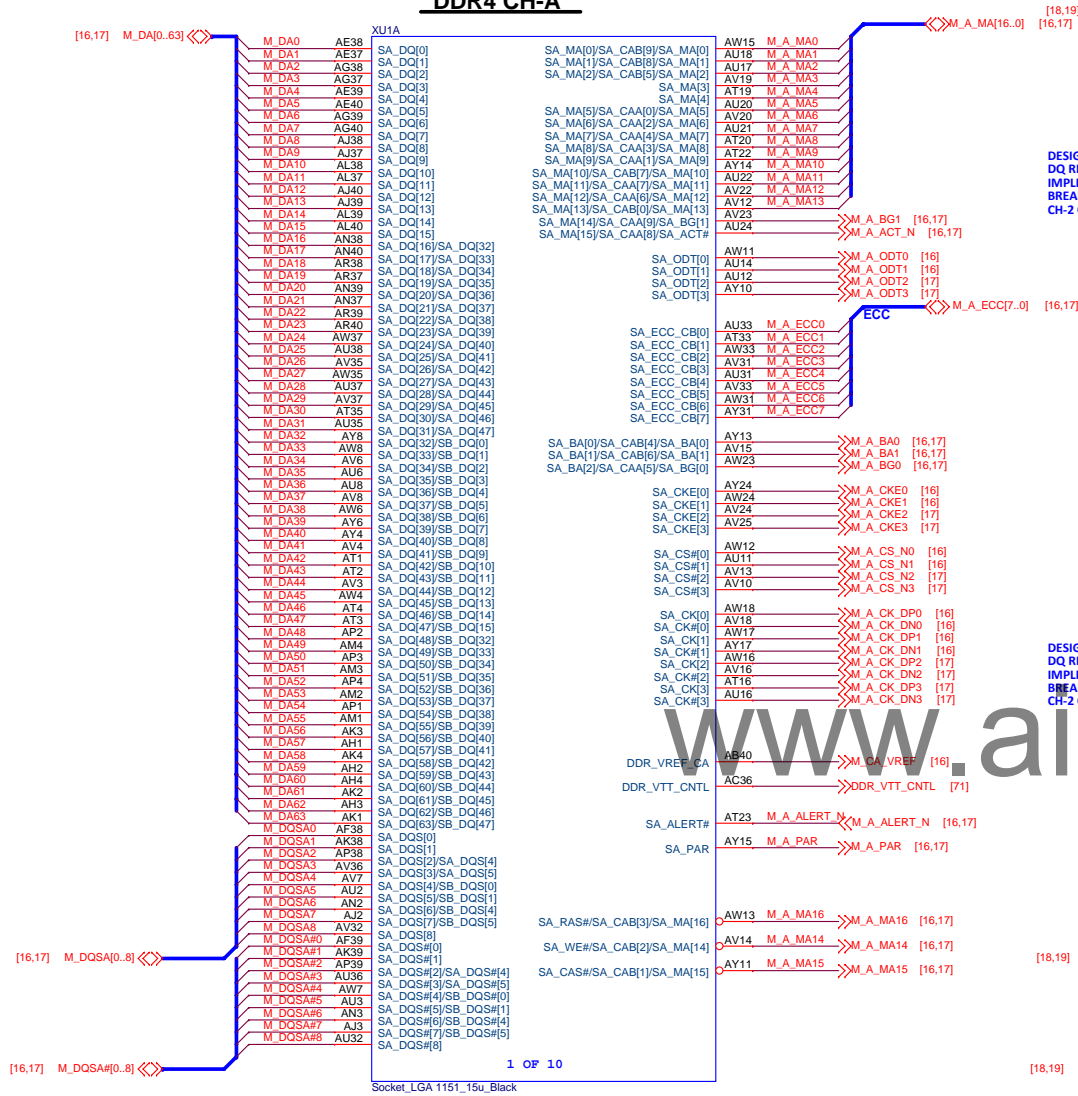
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 Tu-cheng City, Taipei Hsien, Taiwan, R.O.C Fax: 886-2-7705-7901

Title: **MCP- CLK/ CTRL/ MISC/DEBUG**

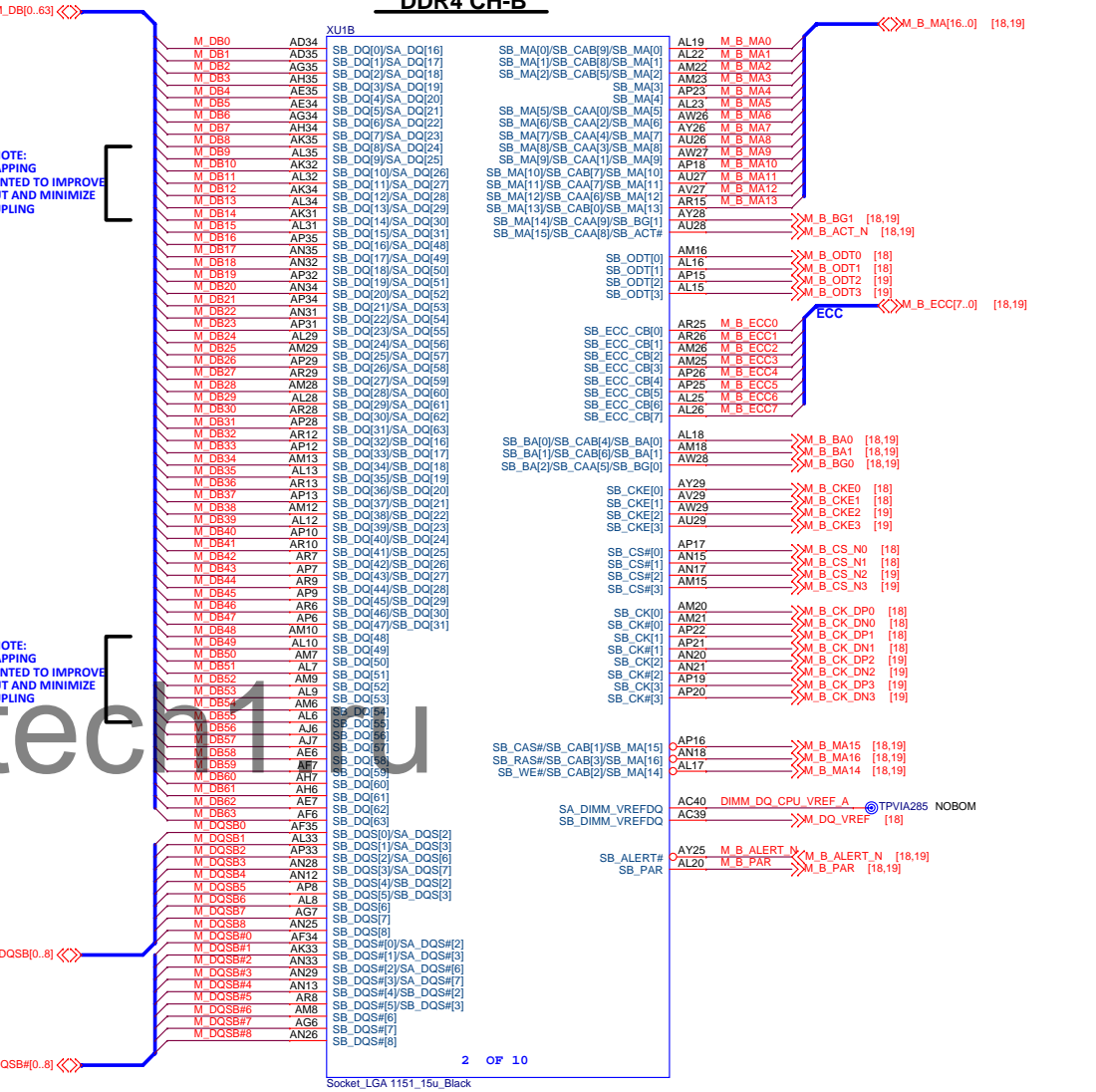
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## DDR4 CH-A

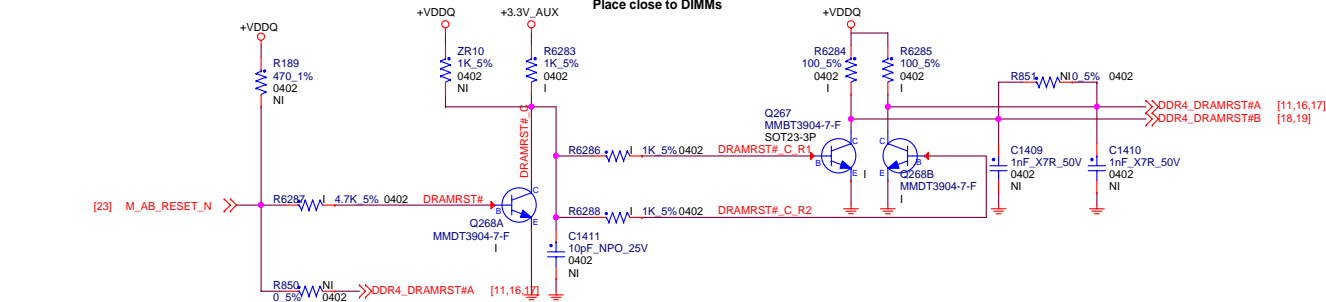


## DDR4 CH-B



## DDR4 DRAMRST# BUFFER CIRCUIT

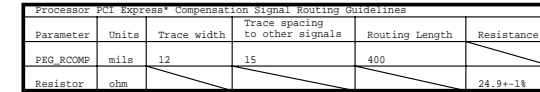
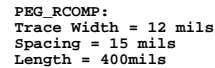
Place close to DIMMs




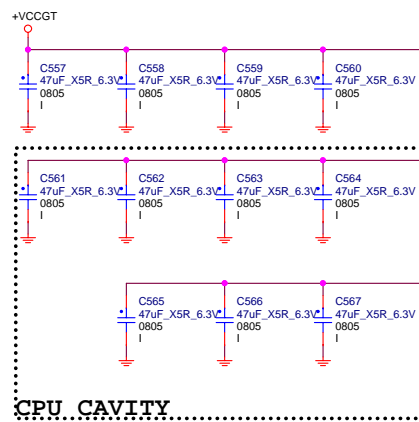
2 OF 10

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PEG AC Cap Value	
Gen1/Gen2	75nf~265nf
Gen3	180nf~265nf

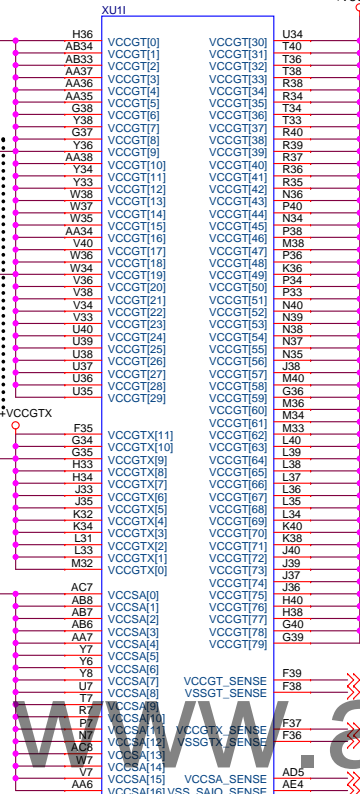


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<b>Title</b>	<b>MCP- PCIE/ DMI/ DD1</b>		
<b>Size</b>	<b>Document Number</b> <b>Skylake_Ataylor</b>		<b>Rev</b>
<b>Page Modified: Thursday, August 06, 2015</b>		<b>16:17:59 (UTC/GMT)</b>	<b>Sheet 12 of 74</b>

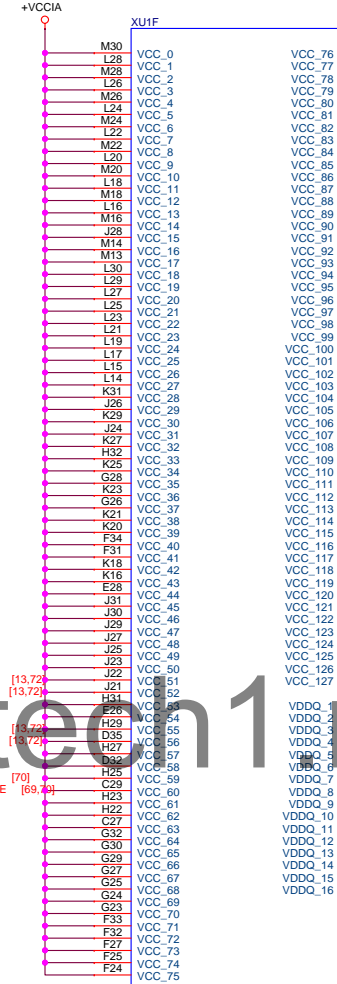


CPU CAVITY

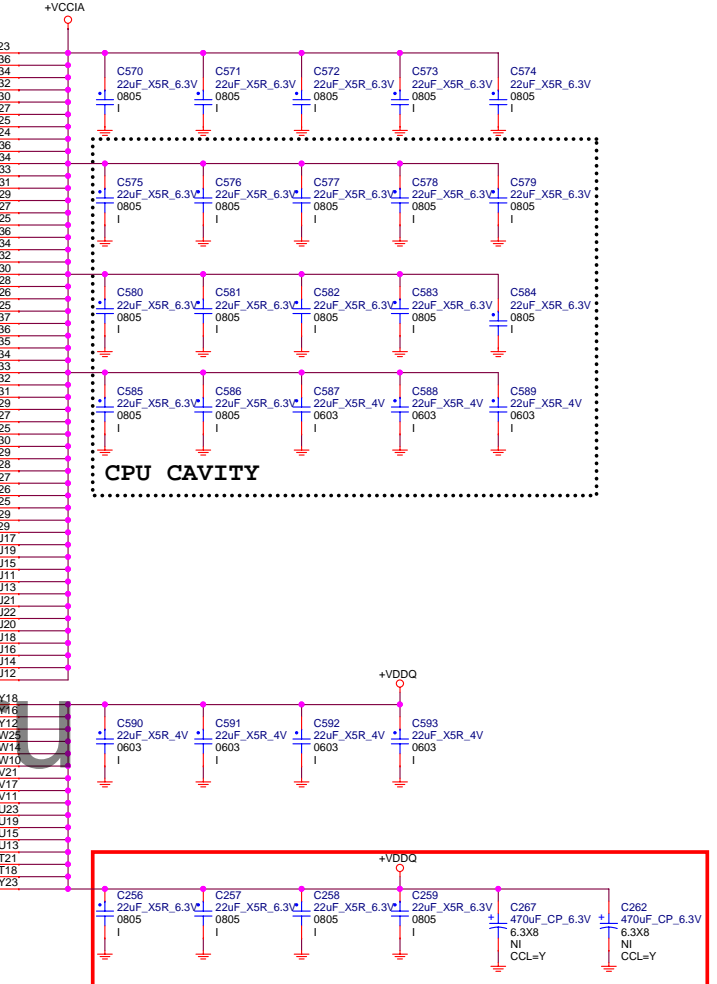
DVT move to power portion



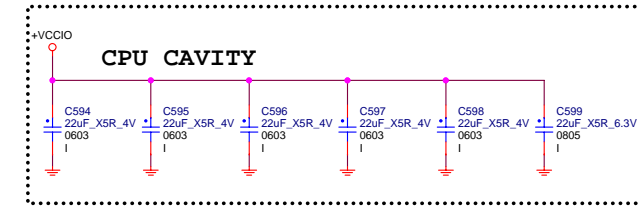
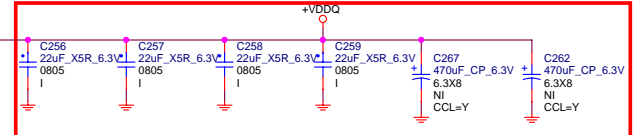
9 OF 10  
Socket\_LGA 1151\_15u\_Black



6 OF 10  
Socket\_LGA 1151\_15u\_Black



Place between 1st DIMM and CPU



CPU CAVITY

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Title <b>MCP-VCC/VDDQ</b>		
Size Custom	Document Number <b>Skylake_Atayal</b>	Rev <b>B</b>
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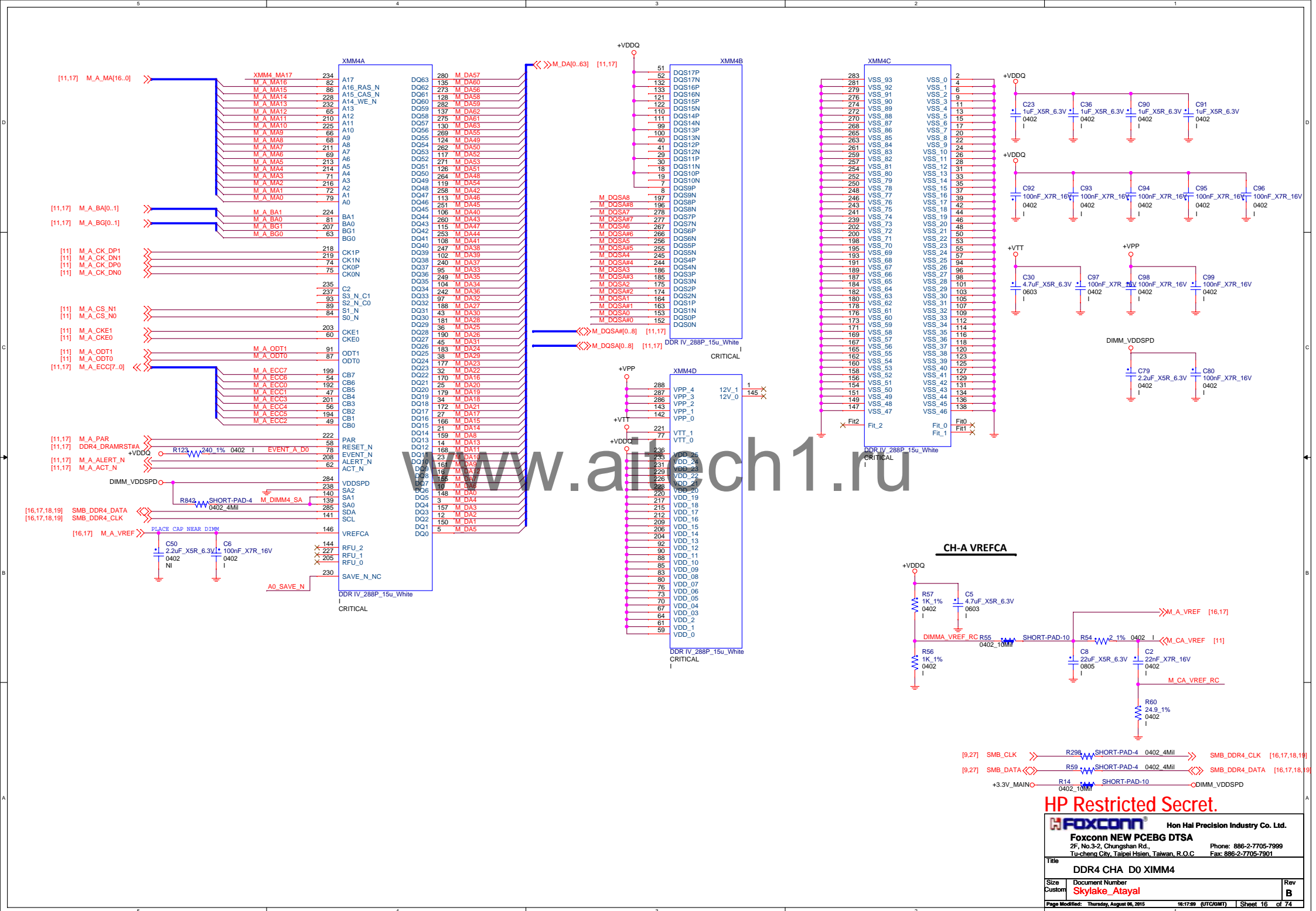
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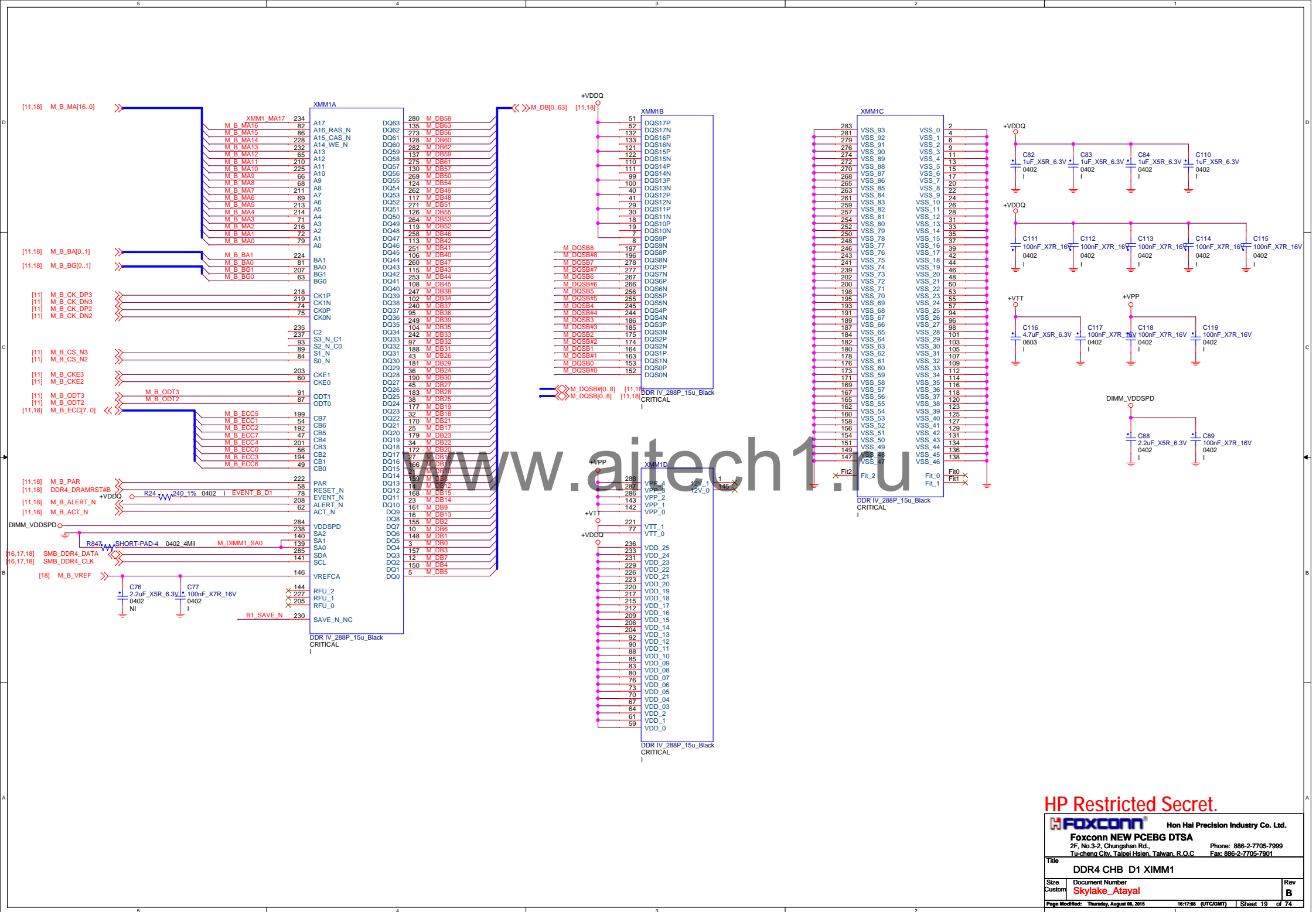
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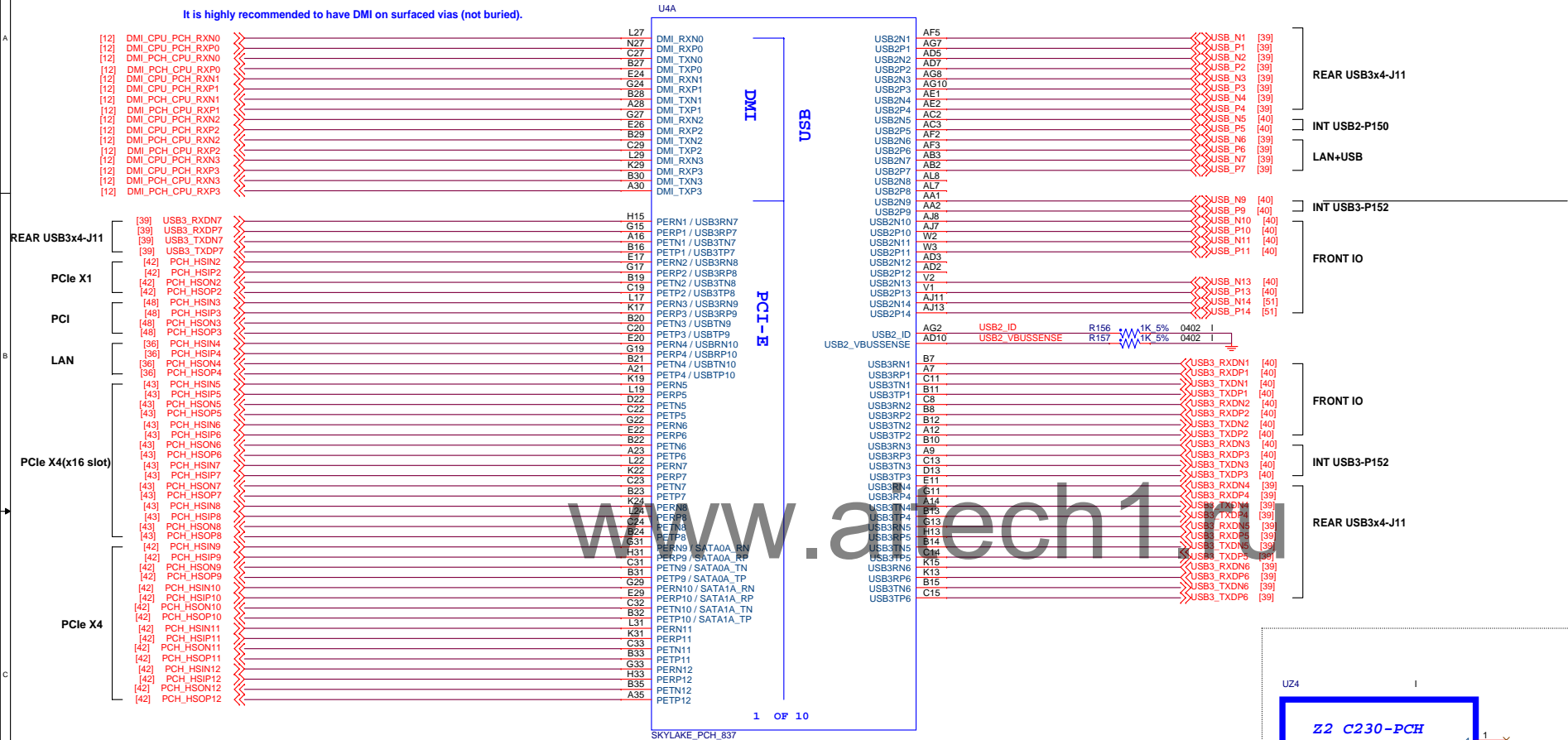




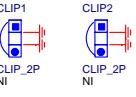
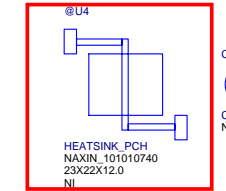
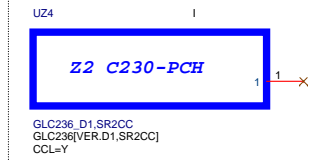
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It is highly recommended to have DMI on surfaced vias (not buried).

It is highly recommended to have DMI on surfaced vias (not buried).

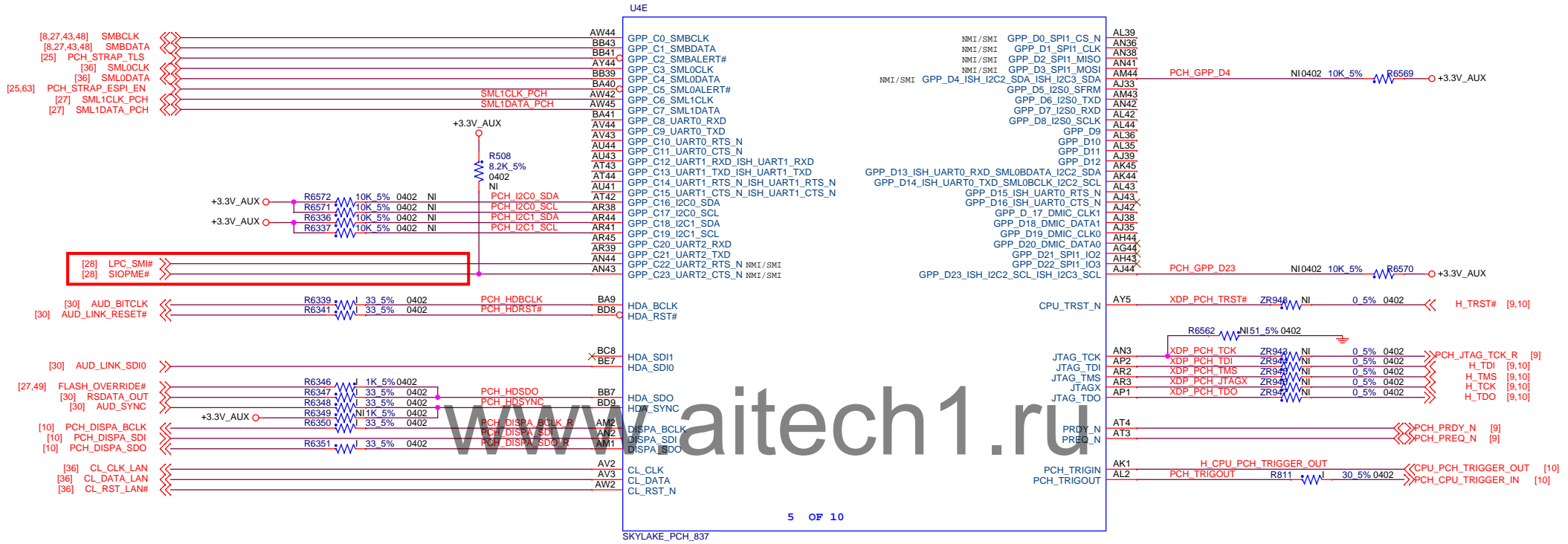


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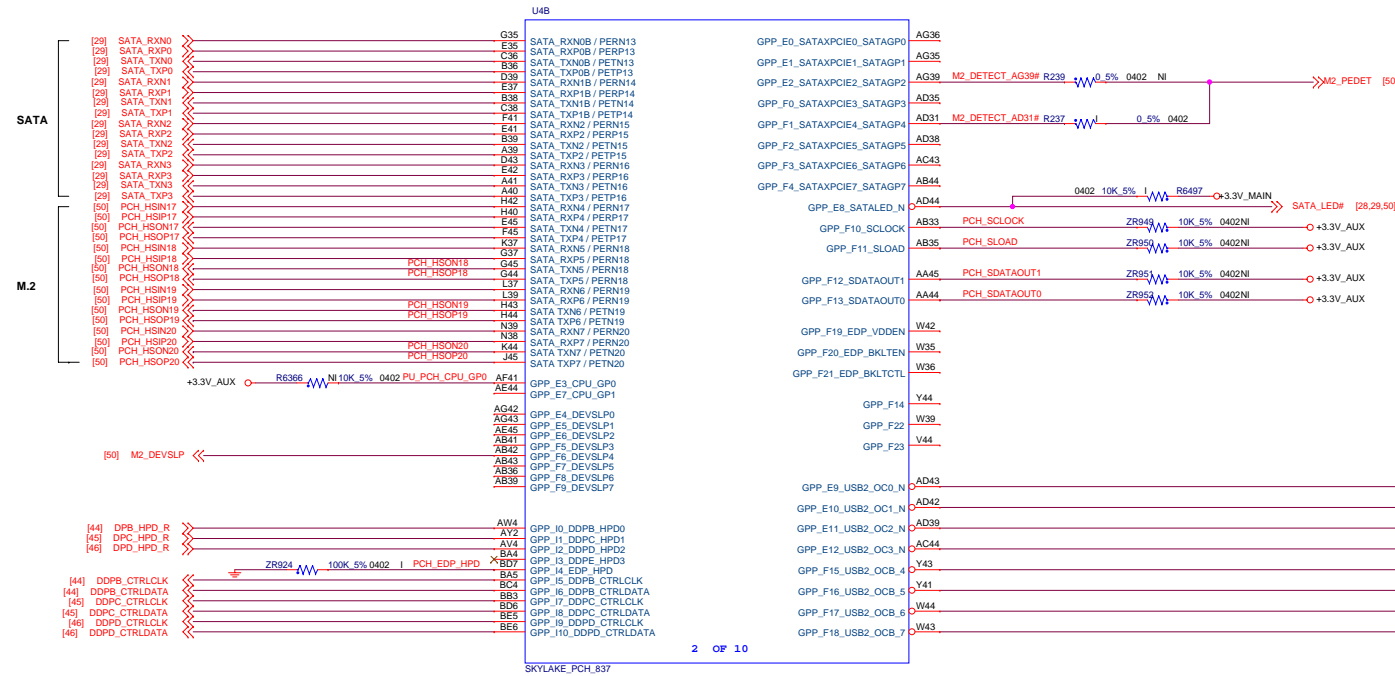
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Phone: 886-2-7705-7999		Fax: 886-2-7705-7901	
Title: PCH - DMI/ PCIE/ USB2/3			
Size: Custom	Document Number: Skylake_Atayal	Rev: B	
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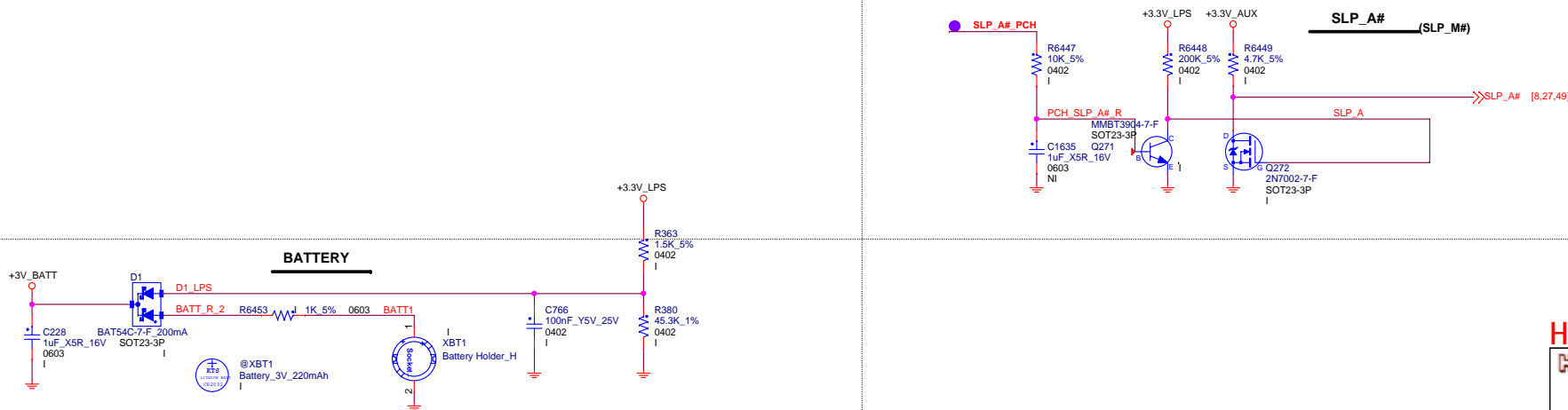
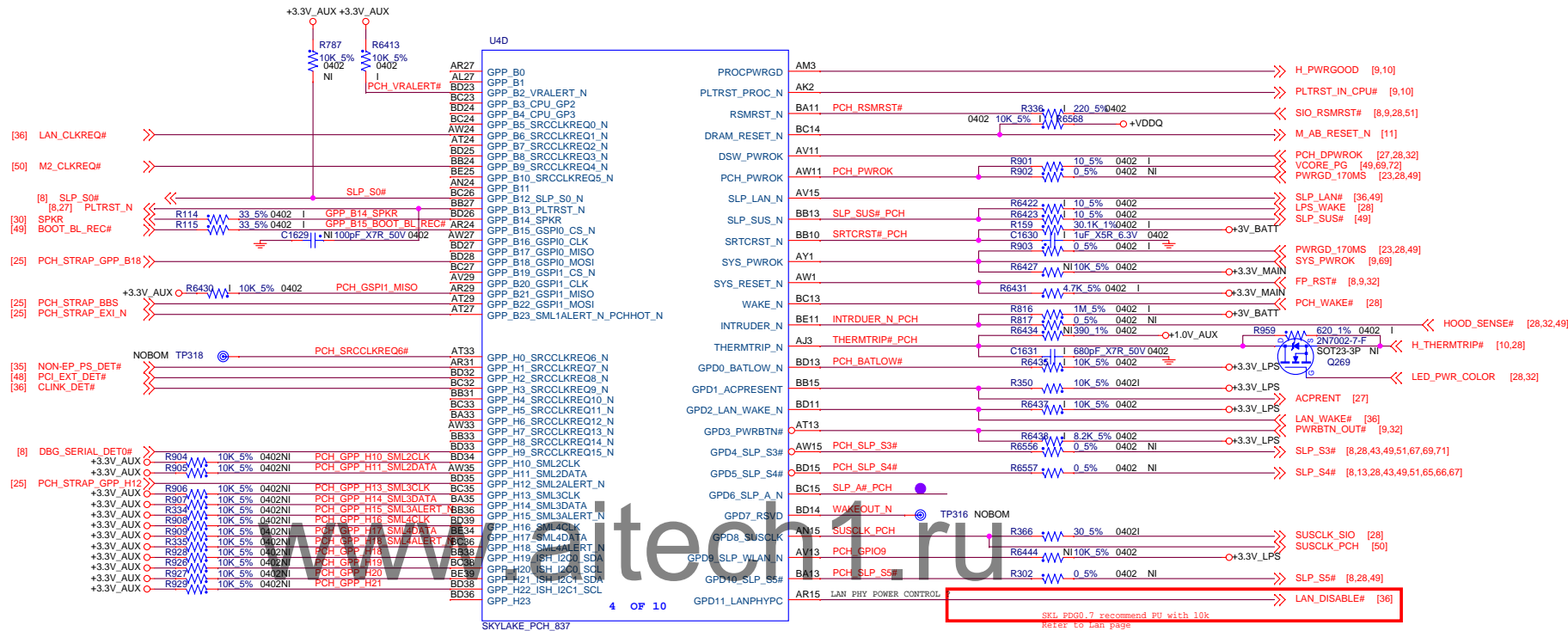


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Title <b>PCH - SMBUS/HDA/GPIO</b>			
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<b>Title</b> PCH - GPIO/MISC		
<b>Size</b> Custom	<b>Document Number</b> SkyLake_Atayal	<b>Rev</b> B
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## U4C



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**Fax: 886-2-7705-7901**

<b>Title</b>	
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PCH - CLOCK

Size

Document Number

29

Cust

Skylake\_Atayal

3

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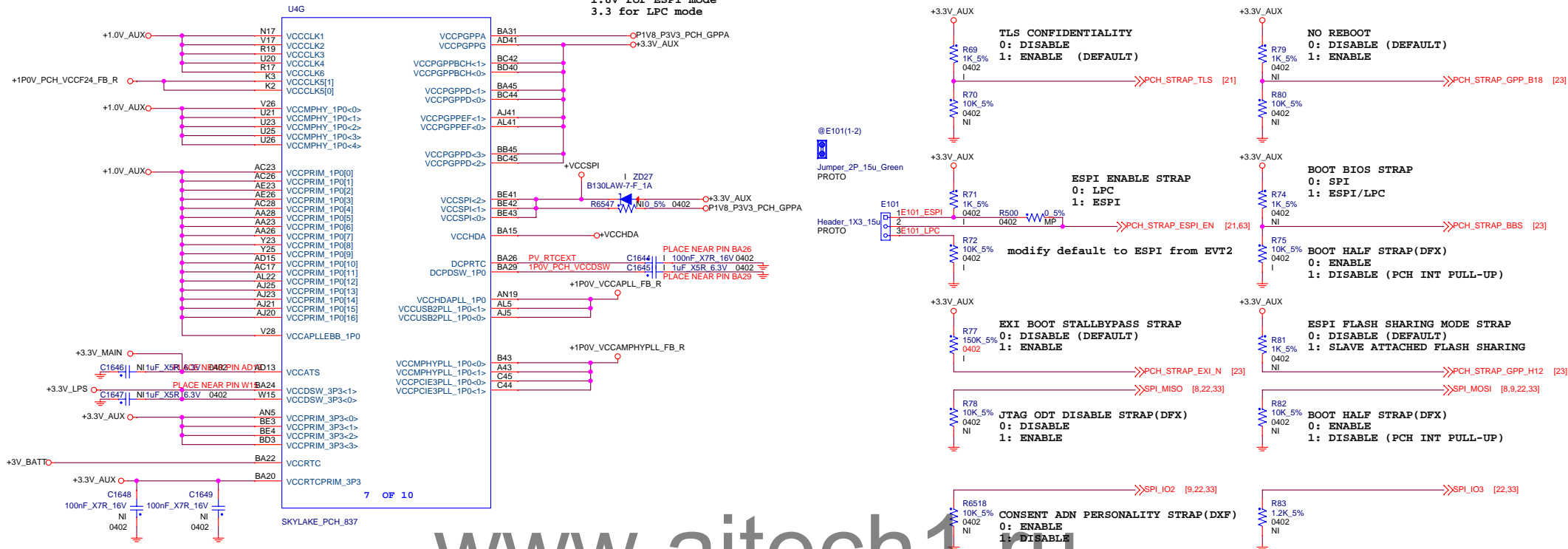
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8





P1V8\_P3V3\_PCH\_GPPA  
1.8V for ESPI mode  
3.3 for LPC mode



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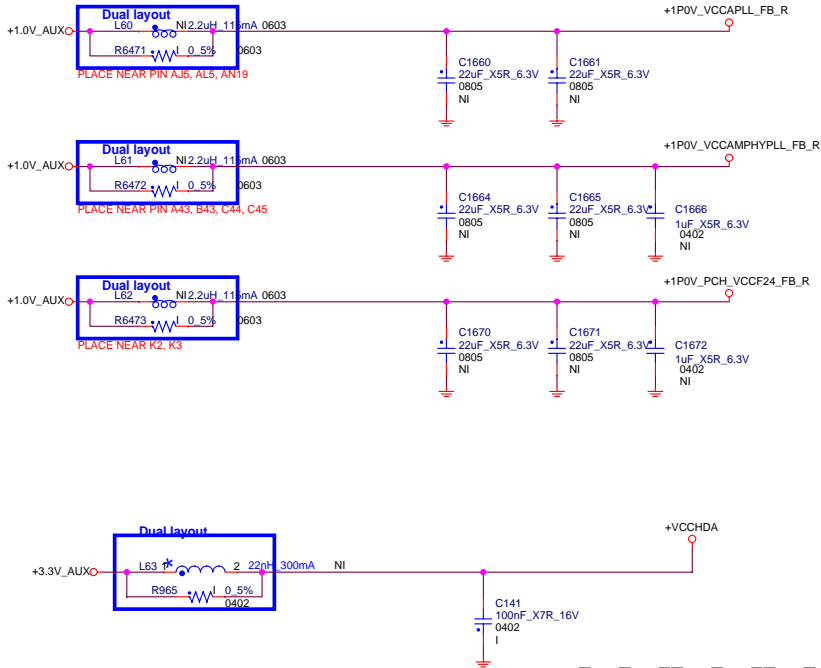
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Size	Document Number	Rev
Custom	Skylake_Atayal	B

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SKYLAKE Decoupling & filter

FILTER

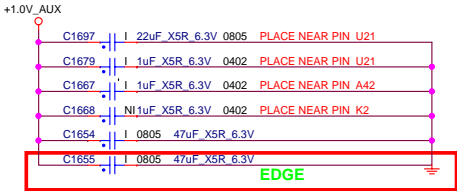


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Power Plane Isolation

Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14 W14 AB2
	SSC	T16, V16 AA16, W16
	USB2	AF19, AF20, AF22, AF23, AP22
PCH 3.3V Standby	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
	USB3	P20
	RTC	AP35
PCH 3.3V	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVCMOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26

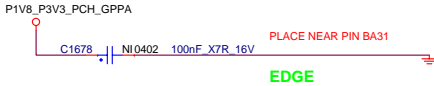
V1.0A



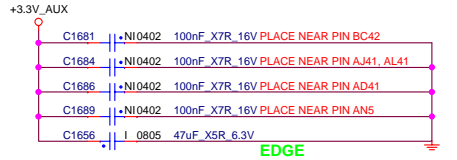
V3.3 DSW



VccPGPPA



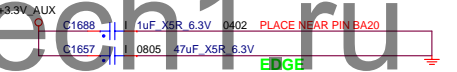
V1.8A / V3.3A



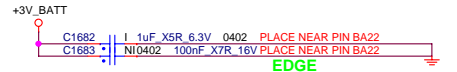
V1.8A / V1.8S / V3.3S



V3.3A

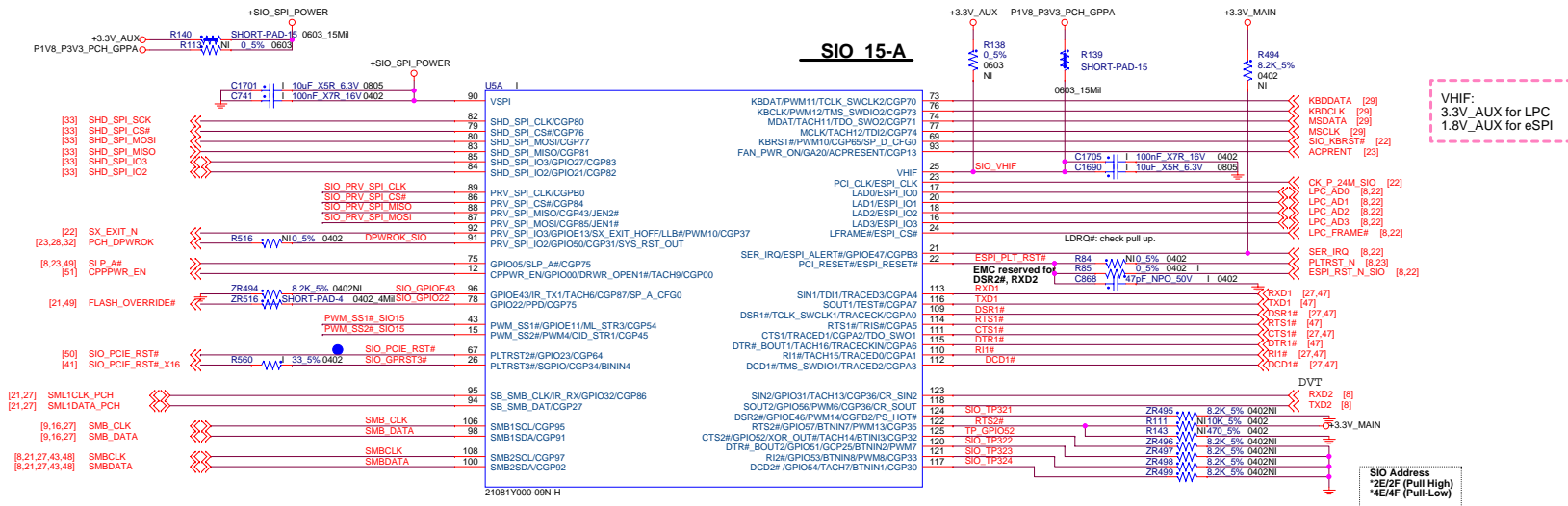


VCCRTC

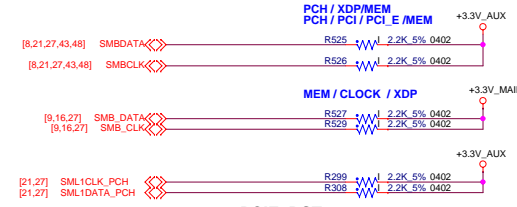


HP Restricted Secret.

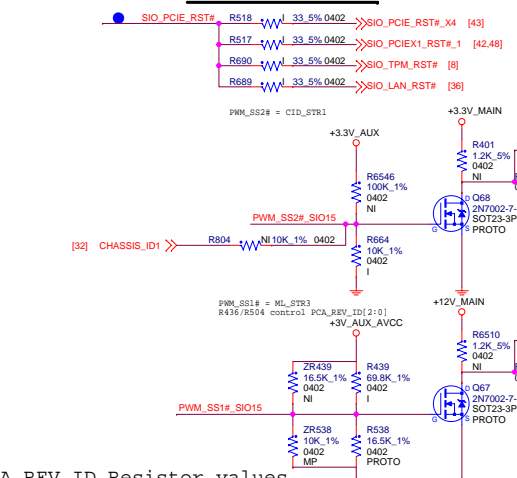
# SIO 15-A



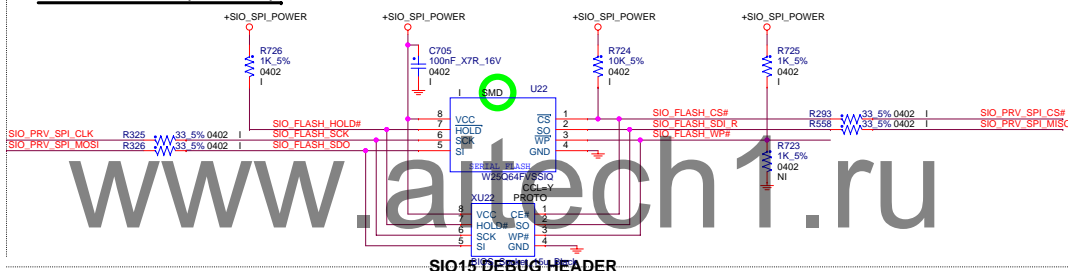
## SM BUS PULL UP



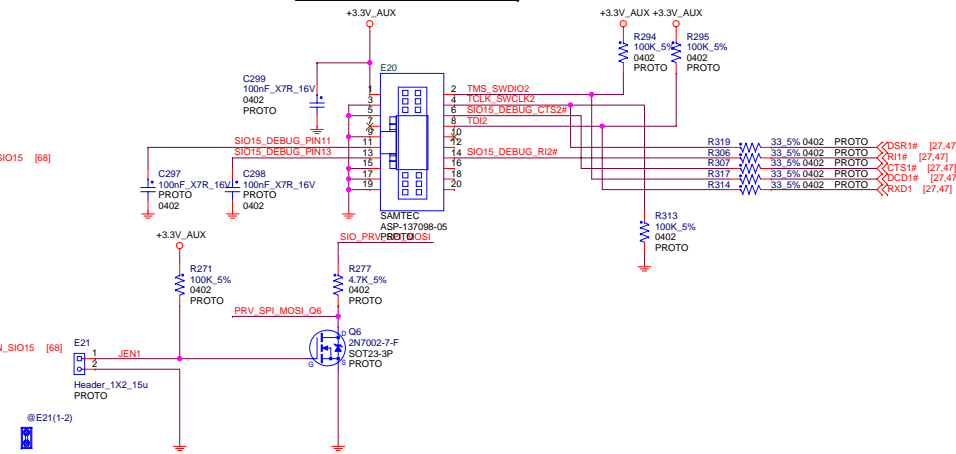
## PCIE\_RST



## SIO Flash ROM (Sure start)



## SIO15 DEBUG HEADER



## PCA\_REV\_ID Resistor values

REV_ID	NP1 WKS	MP	PU 1k	PD 1k	ML_STR3[2:0]b Register Value
0	EVT1	MVB, A	NI	10K	000
1	EVT2	1stECN	69.8K	10K	001
2	EVT3	2ndECN	30.1K	10K	010
3	DVT	3rdECN	16.5K	10K	011
4	PVT1	4thECN	16.5K	16.5K	100
5	PVT2	5thECN	10K	16.5K	101
6	XXX	6thECN	10K	30.1K	110
7	XXX	7thECN	10K	69.8K	111

HP Restricted Secret.

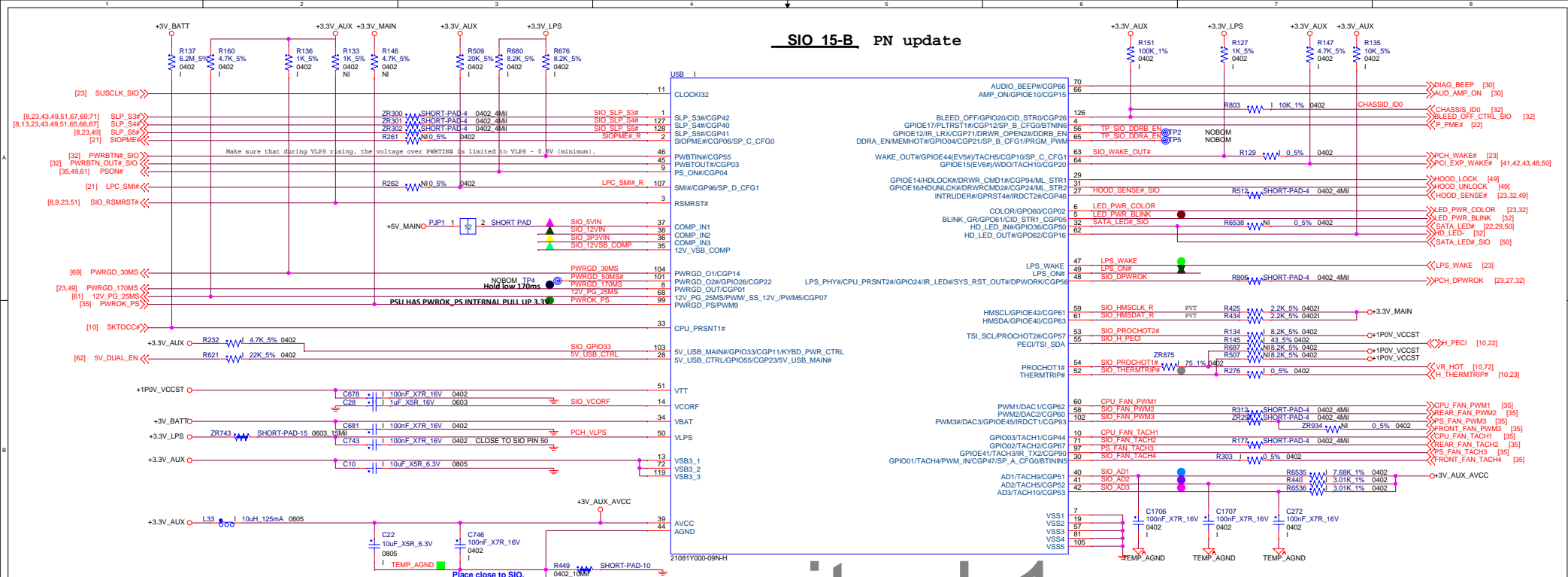
**Foxconn** Hon Hai Precision Industry Co. Ltd.  
**Foxconn NEW PCEB DTSA**  
 2F, No.3-2, Chungshan Rd.,  
 Tu-cheng City, Taipei Hsien, Taiwan, R.O.C  
 Phone: 886-2-7705-7999  
 Fax: 886-2-7705-7901

Title: **SIO\_A & Sure start**

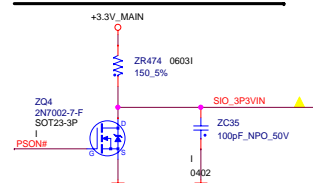
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 Custom: **Skylake Atayal**

Page Modified: Thursday, August 05, 2015 16:17:28 (UTC/GMT) Sheet 27 of 76

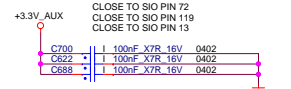
SIO 15-B PN update



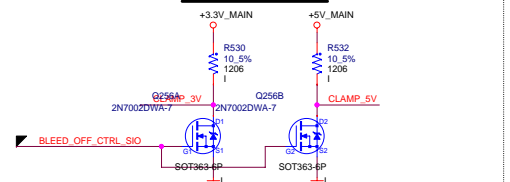
**SIO15- For FIX Sure Start issue**



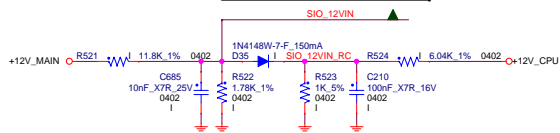
### SI015- SIO Input Power Decoupling Cap



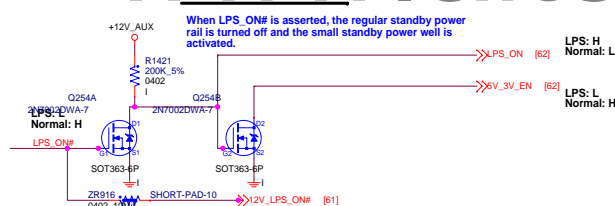
**CLAMP\_CTRL 3.3V / 5V**



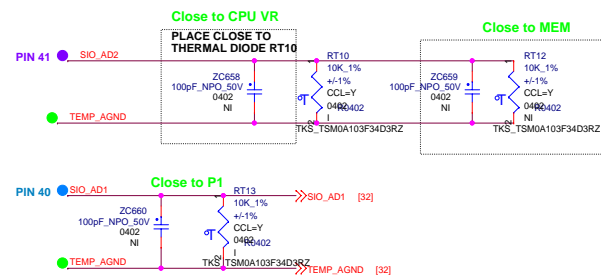
**COMPARATOR INPUT 2 - 12V**



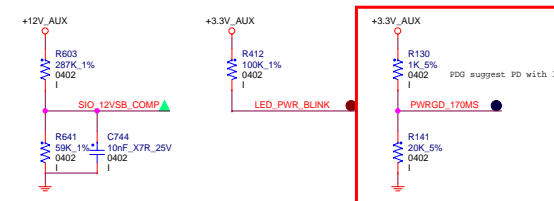
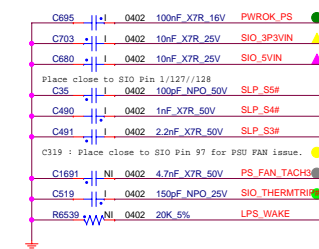
## LPS ON# / LPS ON



### TEMP SENSOR ( SIO15)



### SIO15- SIO Critical Signal PU/PD + Decoupling



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Hon Hai Precision Industry Co. Ltd

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Phone: 886-2-7705-7999  
Fax: 886-2-7705-7001

Title	Super IO-2
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Size	Document Number
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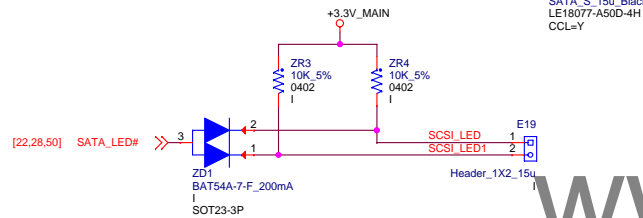
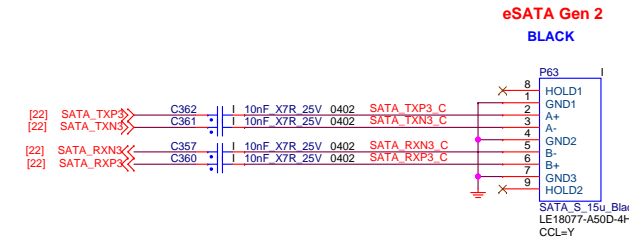
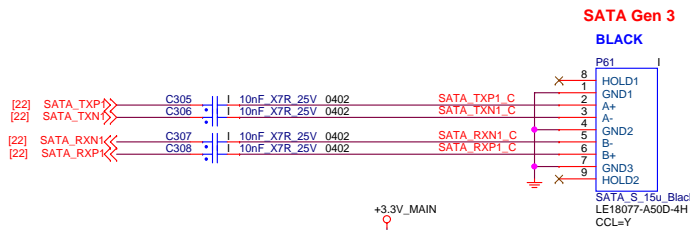
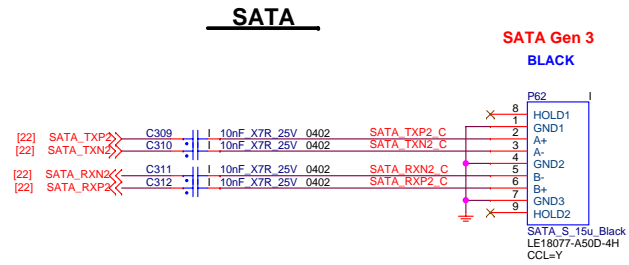
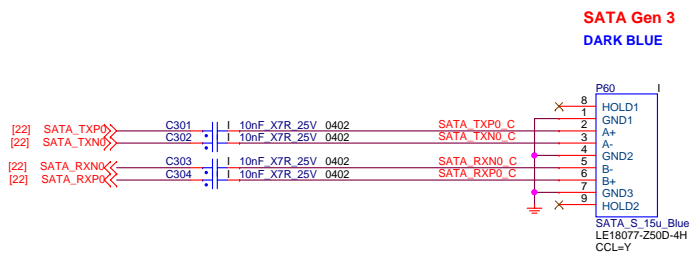
Skylake\_Atayal

Phone: 886-2-7705-7999  
Fax: 886-2-7705-7901

File: 886-Z-7705-7901

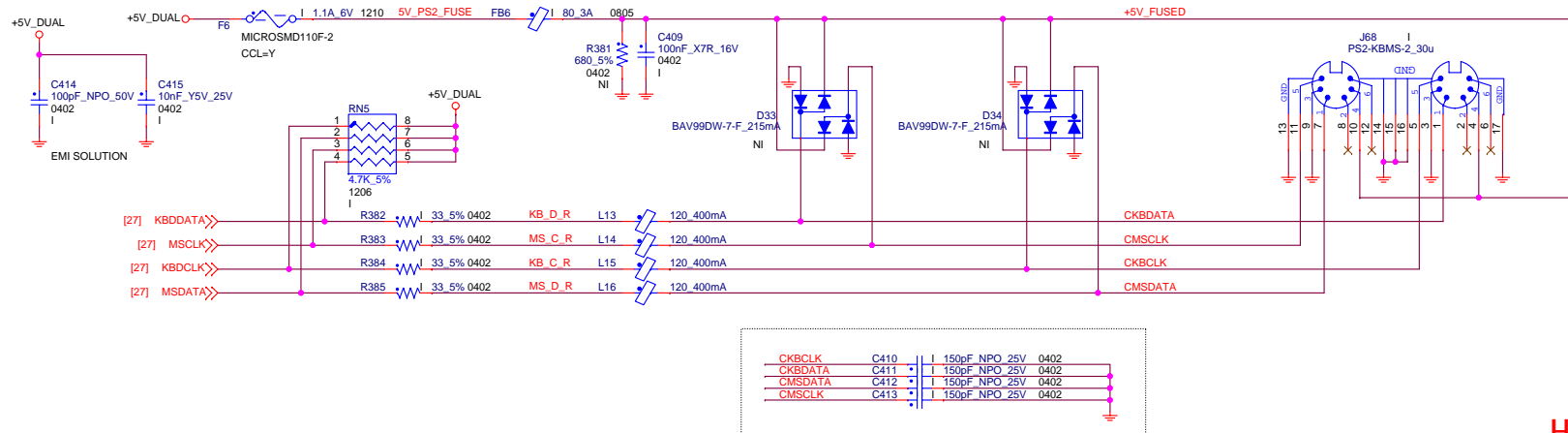
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1000

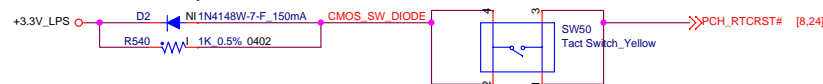


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## PS2 KEYBOARD / MOUSE



## CLEAR CMOS BUTTON



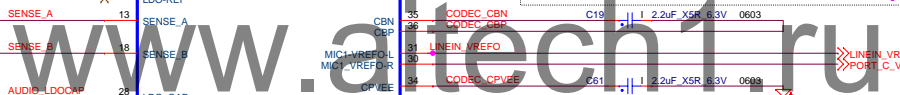
CAD NOTE:  
The PCB must have this  
silkscreen for HPQ

This circuit disables the clear CMOS  
function when system is powered



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## ALC221-VB



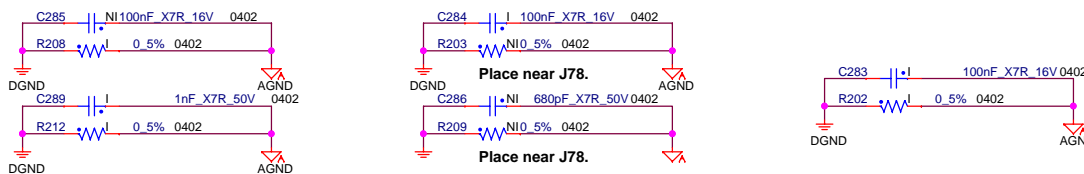
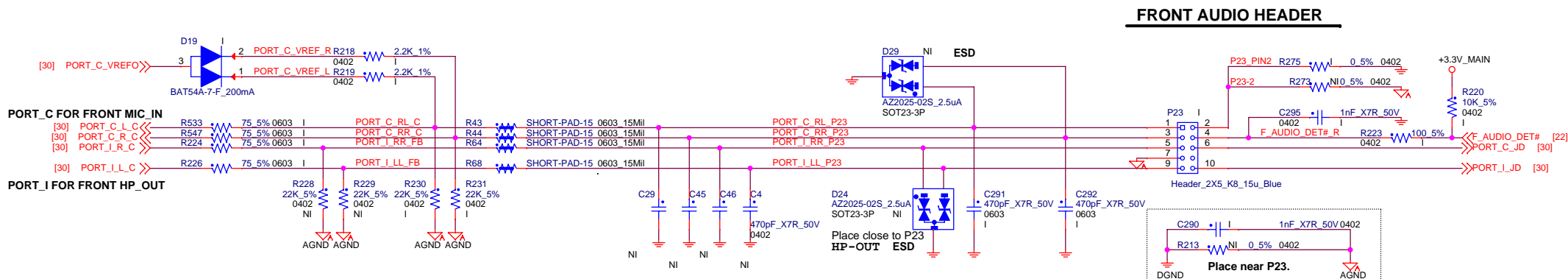
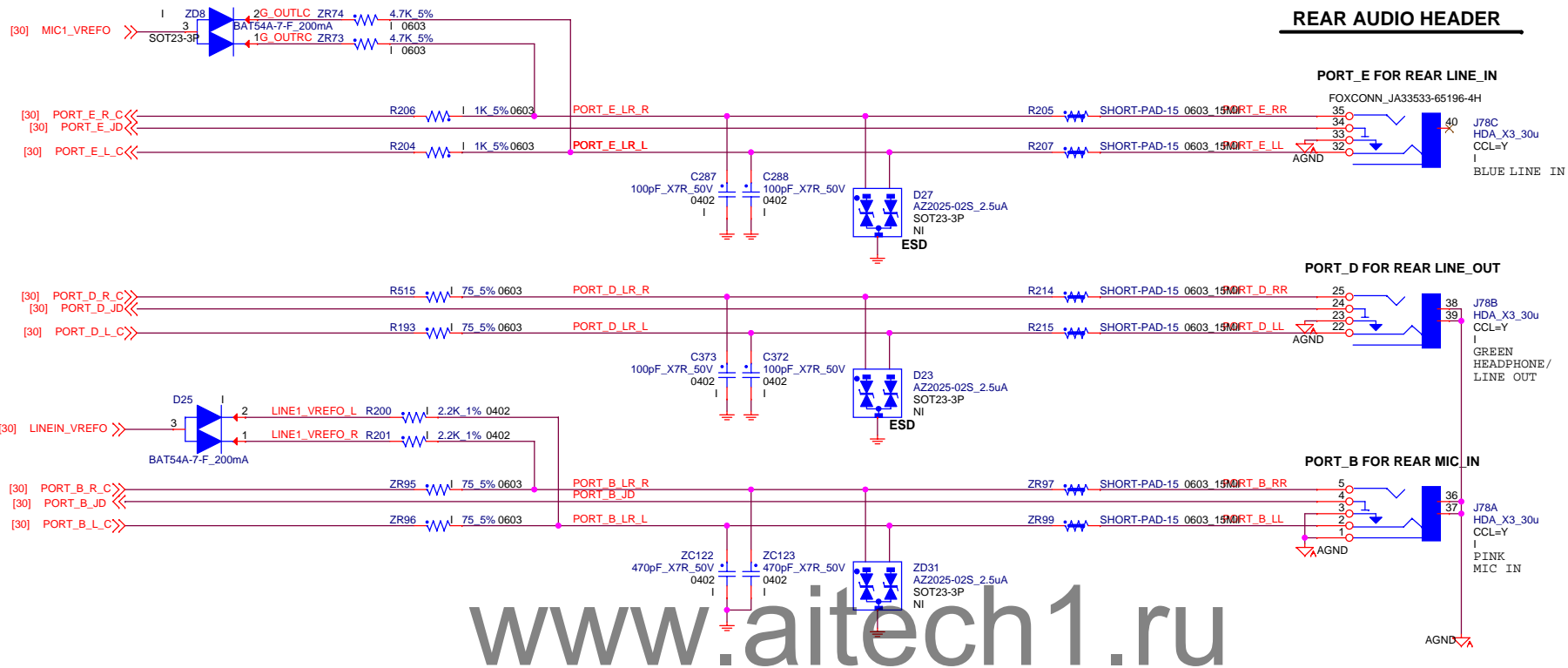
```
Retasking Function

Rear:
Line-in to MIC
MIC      to HP

Front:
MIC      to LINE-in
```

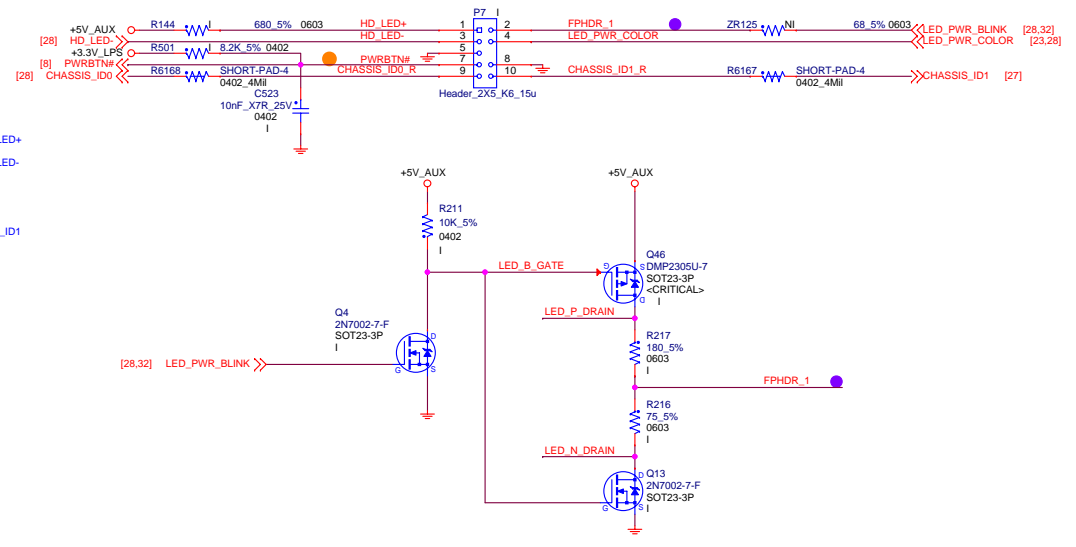
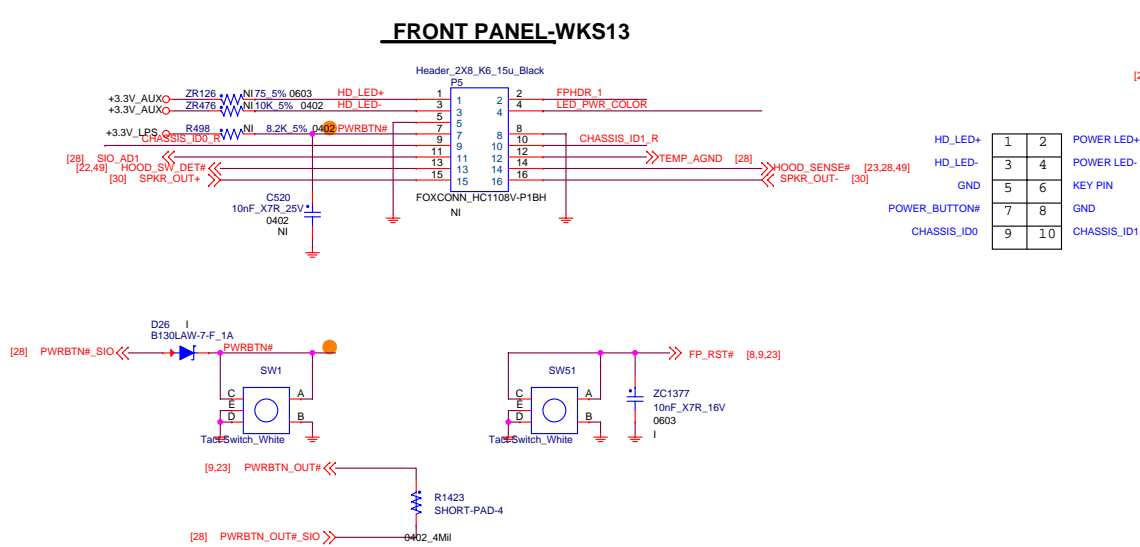
		<b>Hon Hai Precision Industry Co. Ltd.</b>	
<b>Foxconn CMMSSG</b> 2F, No.3-2, Chungshan Rd., Tu-cheng City, Taipei Hsien, Taiwan, R.O.C		Phone: 886-2-7705-7999 Fax: 886-2-7705-7901	
<b>Title</b>			
Super IO-2			
<b>Size</b> Custom		Document Number <b>Skylake Atyal</b>	
Page Modified: Thursday, August 06, 2015		16:17:58 (UTC/GMT) Sheet 30 of 74	



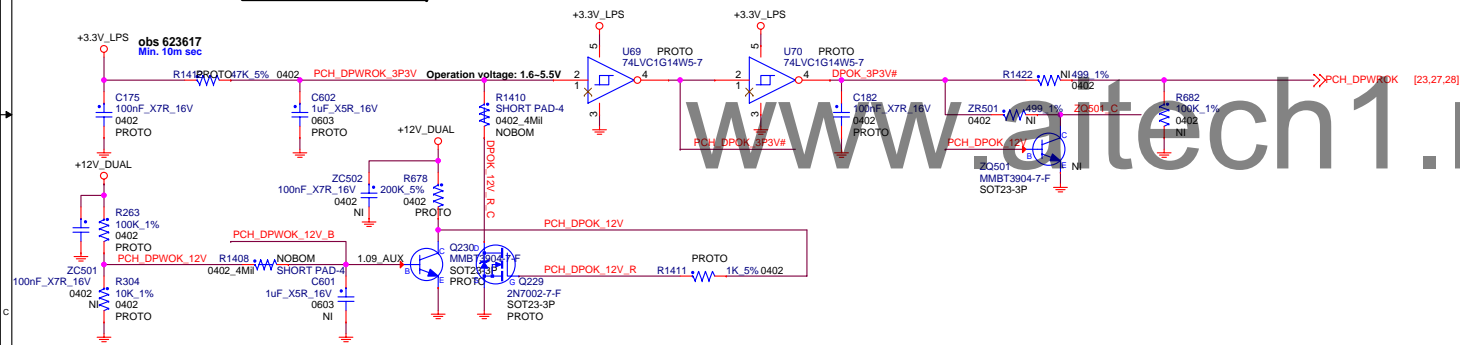


# FRONT PANEL-ENT11

## FRONT PANEL-WKS13

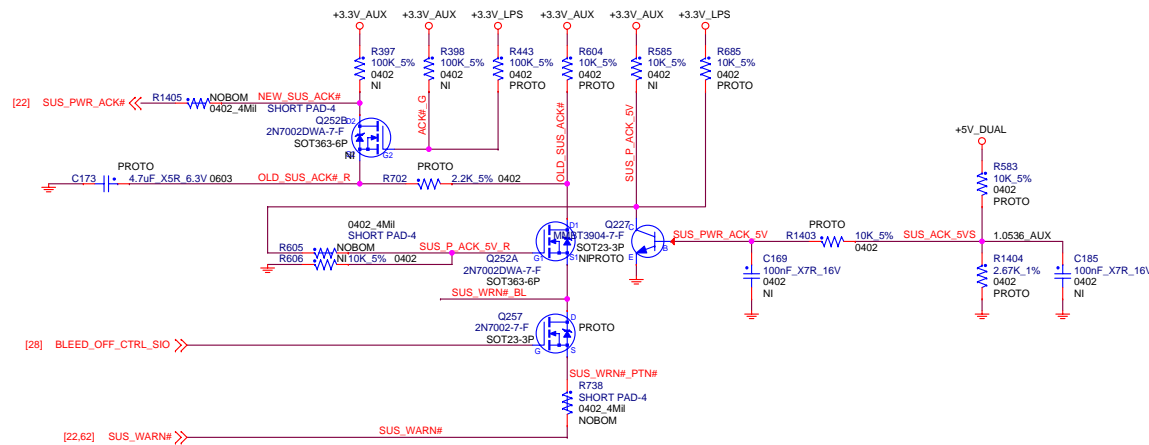


## PCH\_DPWROK



## +5V\_DUAL SUS ACK

DeepSleep Handshake Control Circuit



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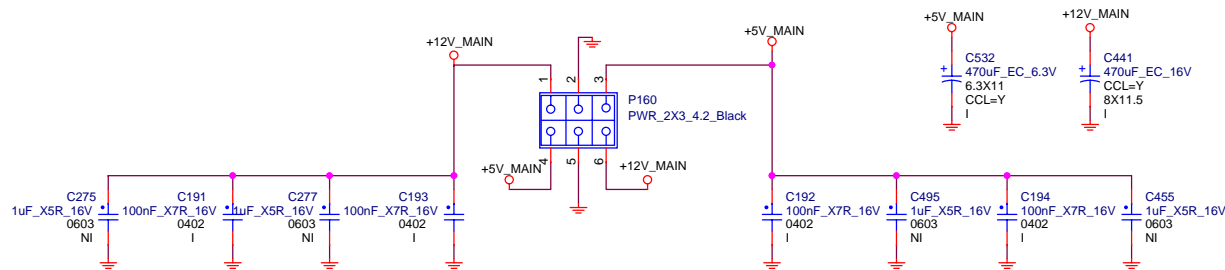




## SATA POWER

## P160 / P161 Bulk cap.

Place closed to P160 / P161



PCB1  
Printed Circuit Board

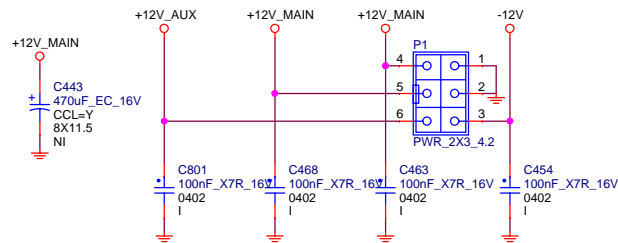
PCB\_REV:1.00

CCL=Y

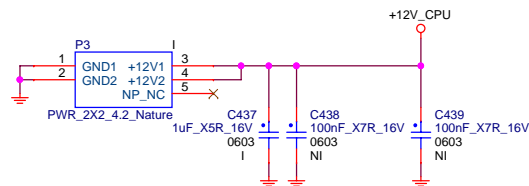
4-Layer PCB, Color With Dark Blue Soldermask, White Silkscreen, NPG-TL, ML1, 9.6X9.8 inch, Rev:1.00, ROHS, HF 0101AR205-35K-H

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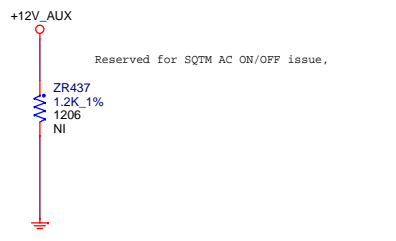
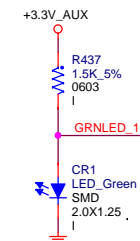
## 12V Power Connector



## VR12V Power Input Connector



## +3V\_AUX LED

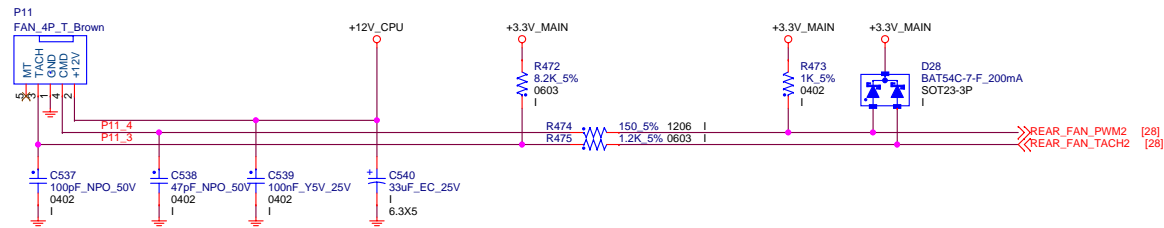


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## Rear Chasis FAN

Color: Red

FAN	PWM	TACH
PSU	3	3
CPU	1	1
FRONT	4	4
REAR	2	2

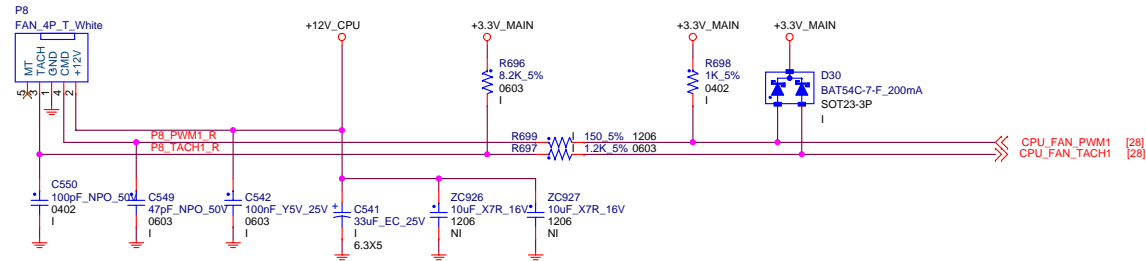


## CPU Fan

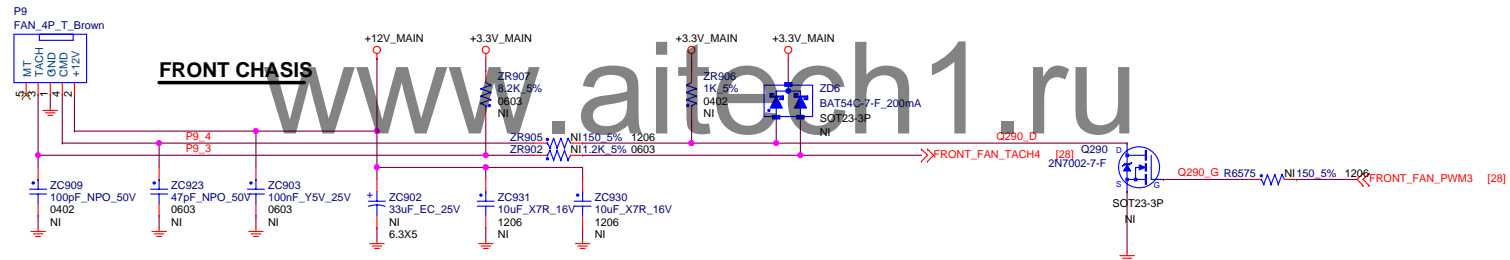
Color: Natural / white

1	GND
2	+12V
3	FAN TACH
4	FAN PWM INPUT

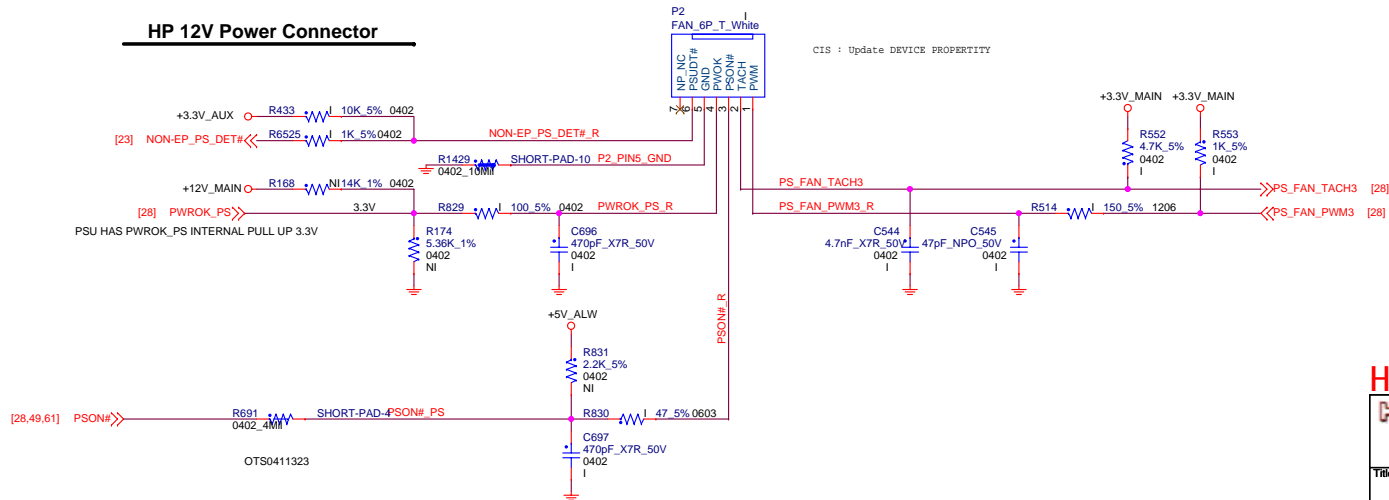
### ZP8 & P8 co-layout



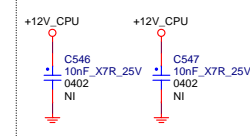
## FRONT CHASIS



## HP 12V Power Connector

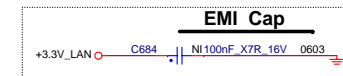
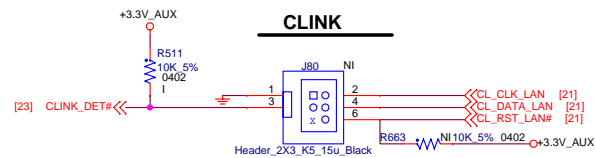
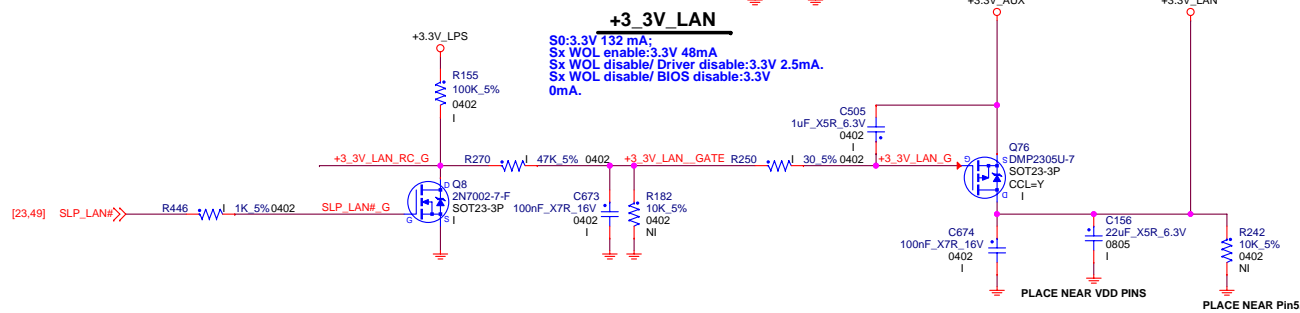
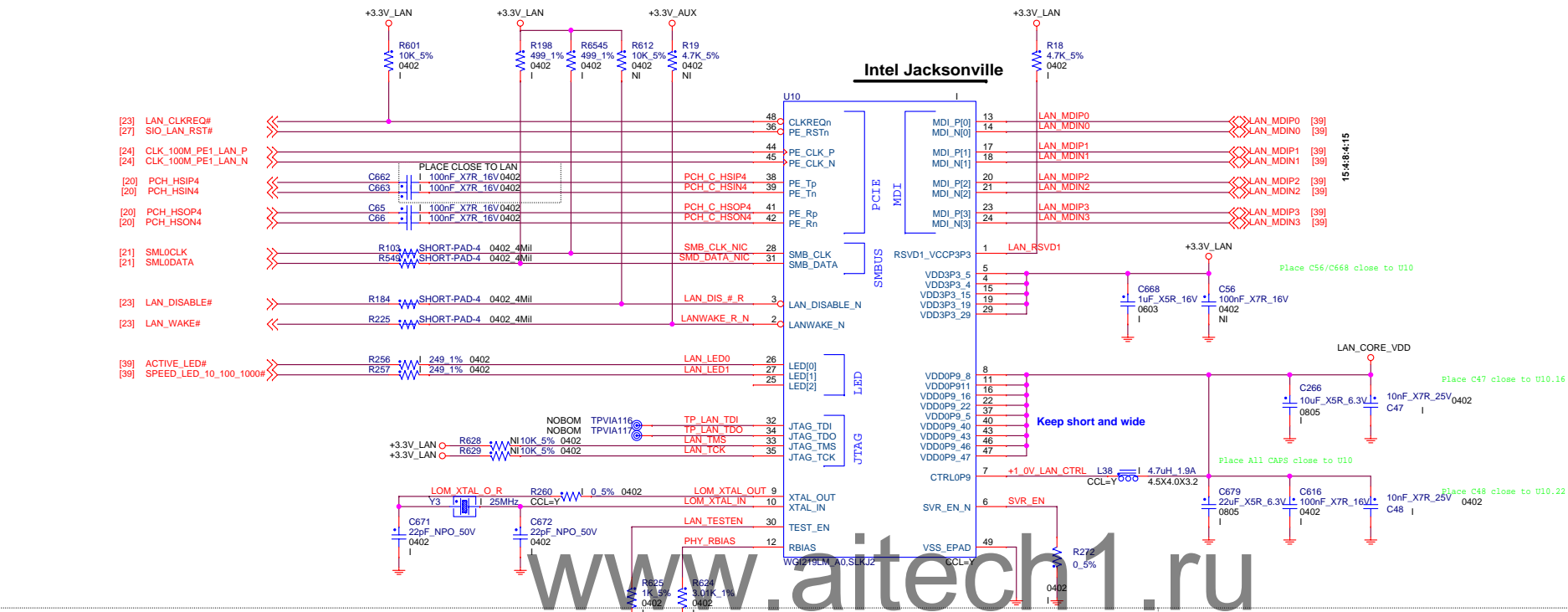


### For EMI




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Title <b>FAN HEADERS, PSU COMMAND/STATUS PIN</b>		
Size Custom	Document Number Skylake_Ataly	Rev <b>B</b>
Page Modified: Thursday, August 06, 2015 18:17:38 (UTC/GMT) Sheet 35 of 76		



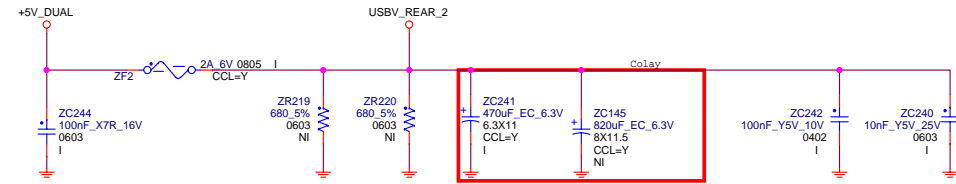
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<b>Foxconn NEW PCEBG DTSA</b>		
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Title NONE		
Size B	Document Number Skylake_Atayal	Rev B
Page Modified: Thursday, August 06, 2015 16:17:08 (UTC+GMT) Sheet 37 of 74		

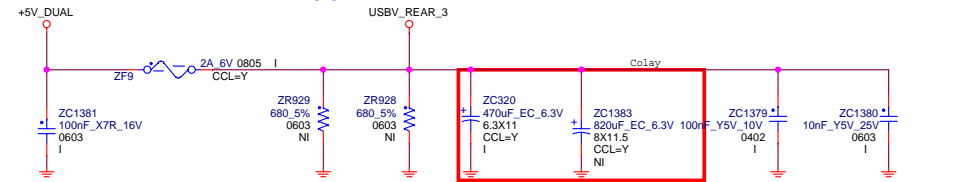
Rear : USB3X4(2ports)  
0.9\*2 = 1.8A

Rear : LAN-USB2(2ports)  
0.5+2 = 1A



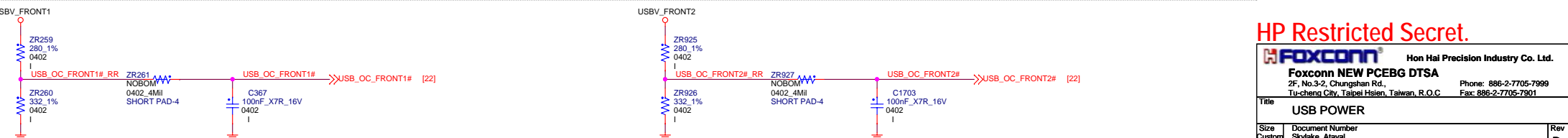
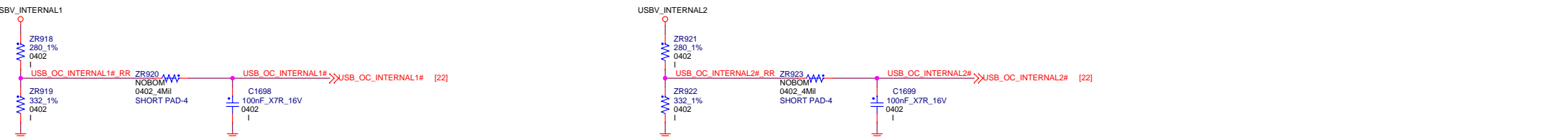
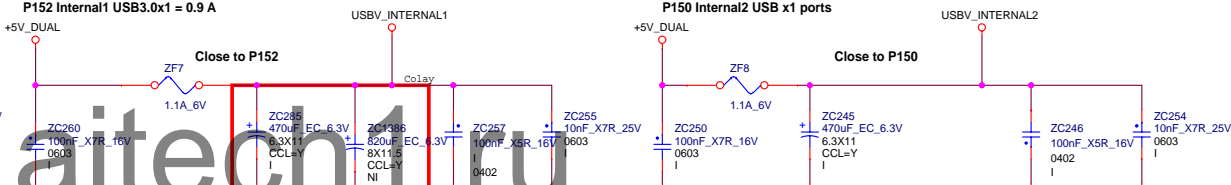
## Internal USB POWER

**P150 Internal2 USB x1 ports**



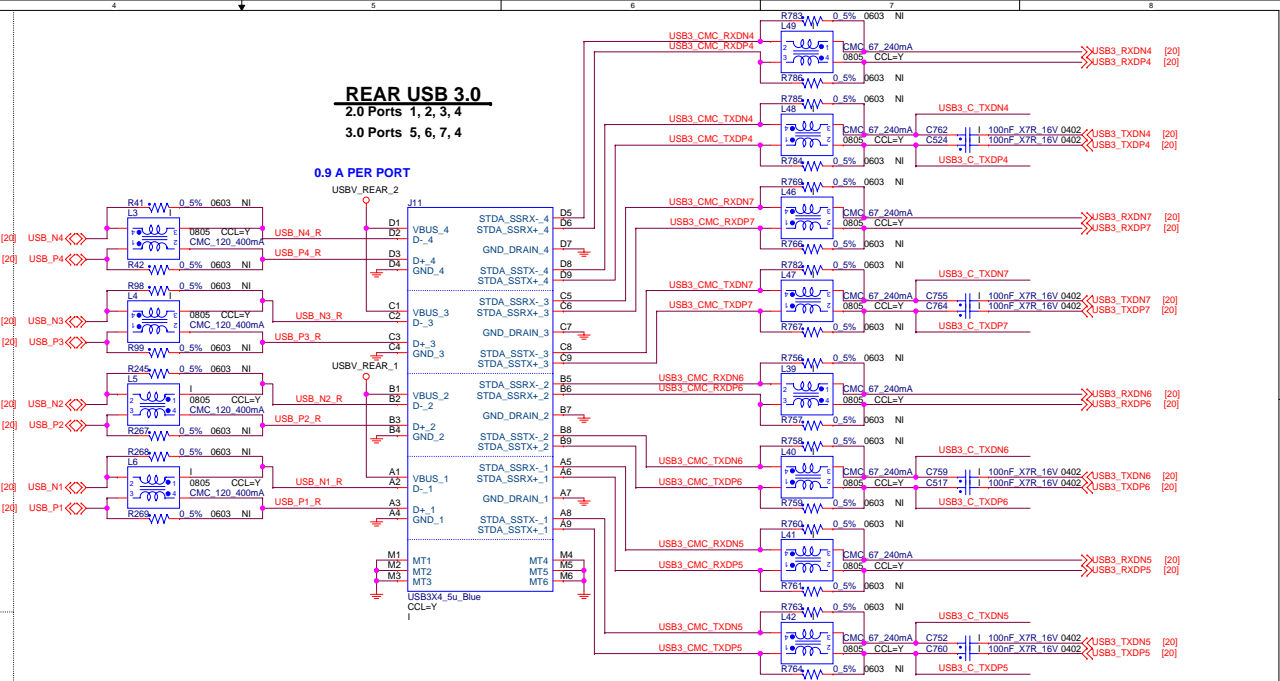
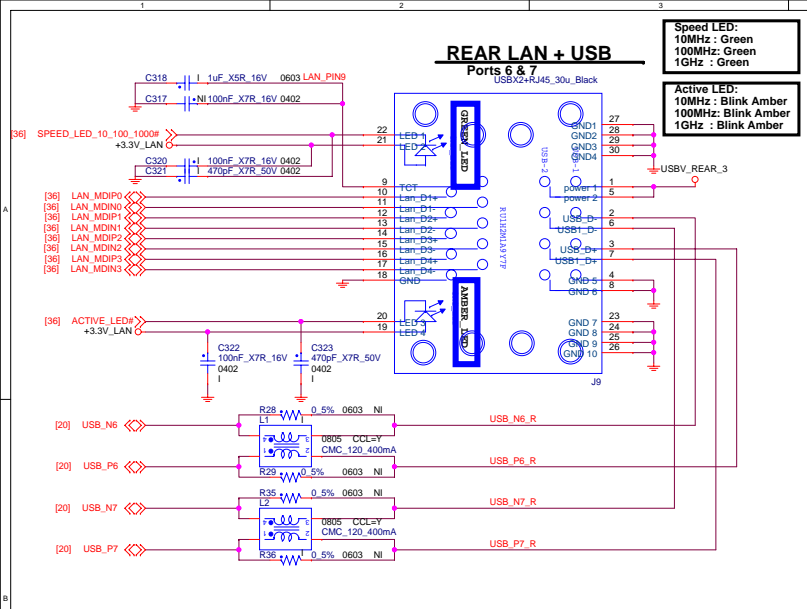
## Internal USB POWER

**P150 Internal2 USB x1 ports**

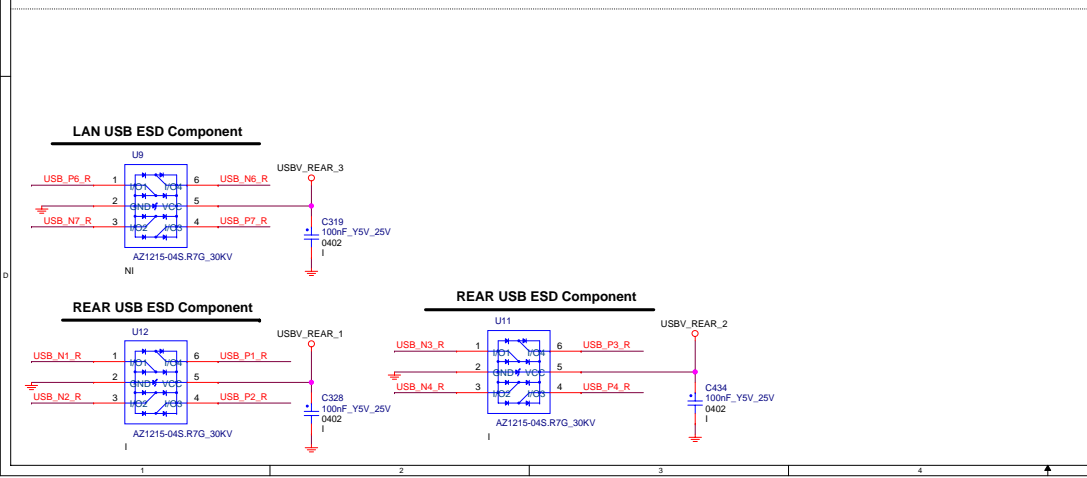
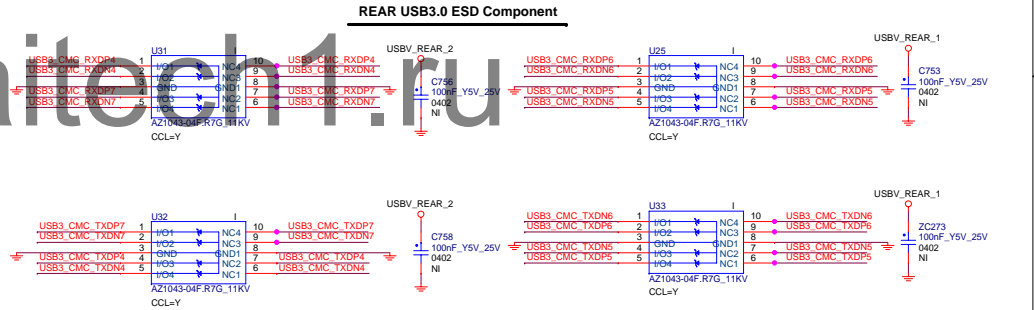


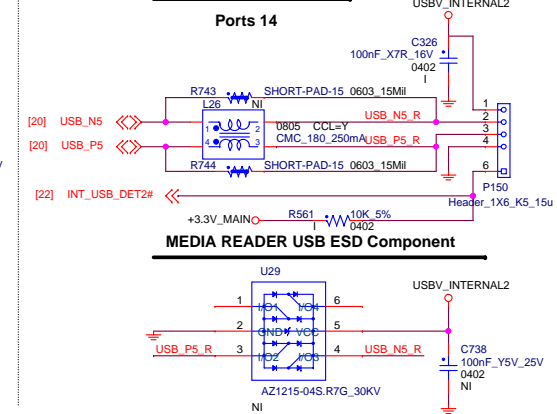
**FOXCONN**<sup>®</sup> Hon Hai Precision Industry Co. Ltd.  
**Foxconn NEW PCEBG DTSA**  
 2F, No.3-2, Chungshan Rd.,  
 Tu-cheng City, Taipei Hsien, Taiwan, R.O.C  
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 Fax: 886-2-7705-7901

Title		10-cheng City, Taipei Dist., Taiwan, R.O.C.		Fax: 886-2-7705-7901	
USB POWER					
Size Custom	Document Number Skylake_Atalay				Rev B
Page Modified:		Thursday, August 06, 2015		16:17:59 (UTC/GMT)	Sheet 38 of 76

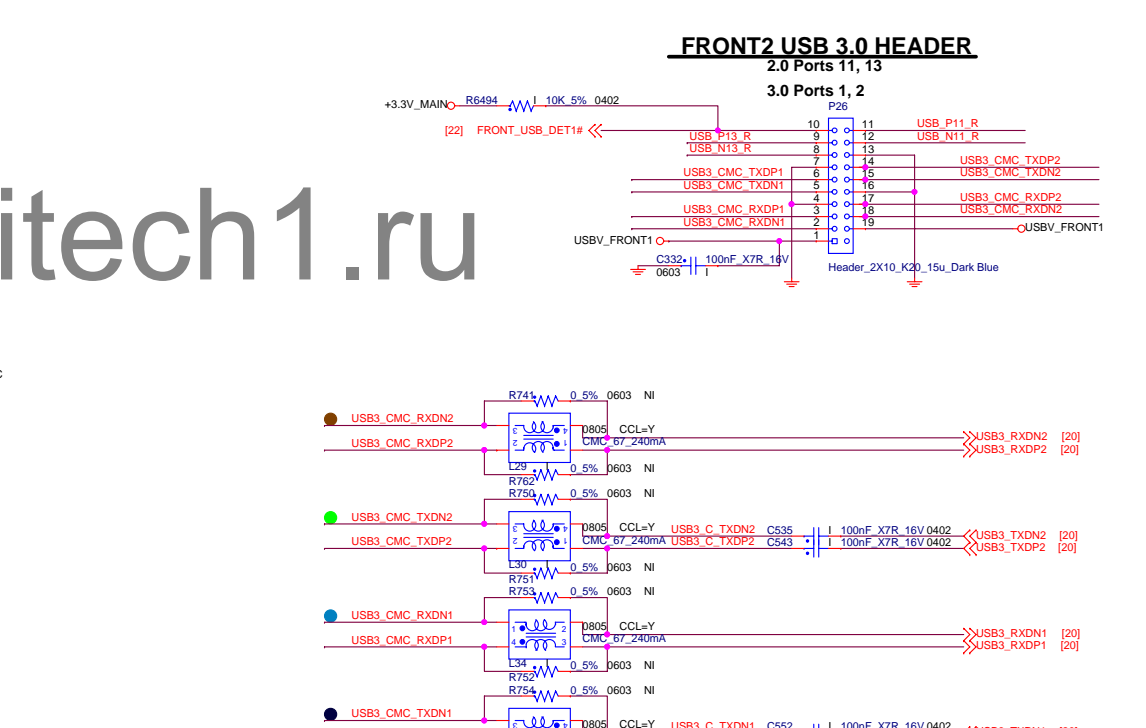


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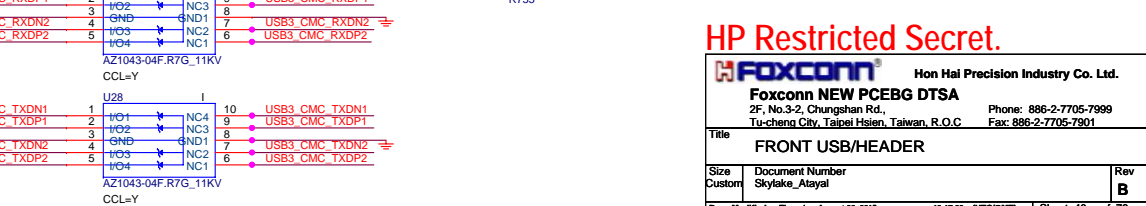


**USB2.0 Ports 9 +USB3.0 Ports 3**

## Port 10&amp;12



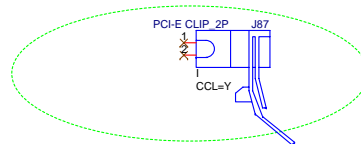
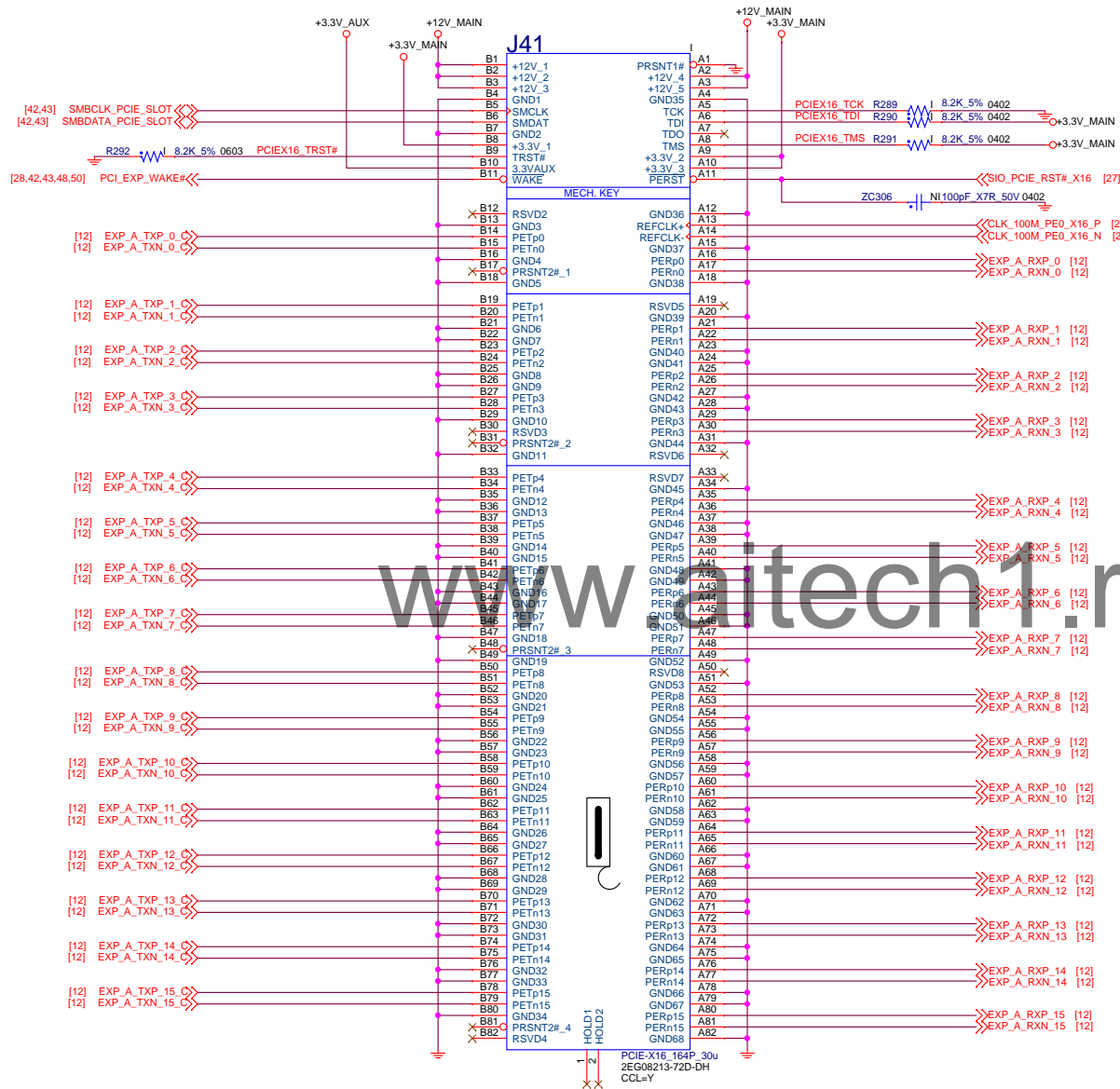
## FRONT2 USB ESD Component



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**Foxconn NEW PCEBG DTSA**  
 2F, No.3-2, Chungshan Rd., Phone: 886-2-7705-7999  
 Tu-cheng City, Taipei Hsien, Taiwan, R.O.C Fax: 886-2-7705-7901



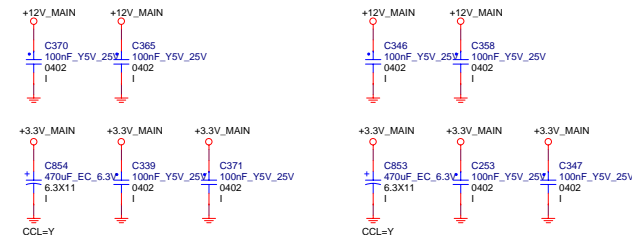
# PCI EXPRESS x16 SLOT 2



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<b>FOXCONN</b> Foxconn NEW PCEBG DTSA 2F, No.3-2, Chungshan Rd., Tu-cheng City, Taipei Hsien, Taiwan, R.O.C.		Hon Hai Precision Industry Co. Ltd. Phone: 886-2-7705-7999 Fax: 886-2-7705-7901	
Title <b>PCIEx16 Slot</b>			
Size	Document Number	Rev	
Custom	<b>Skylake_Atayal</b>	<b>B</b>	
Page Modified: Thursday, August 06, 2015		16:17:36 (UTC+8GMT) Sheet 41 of 76	


## MAIN J31



## MAIN 100

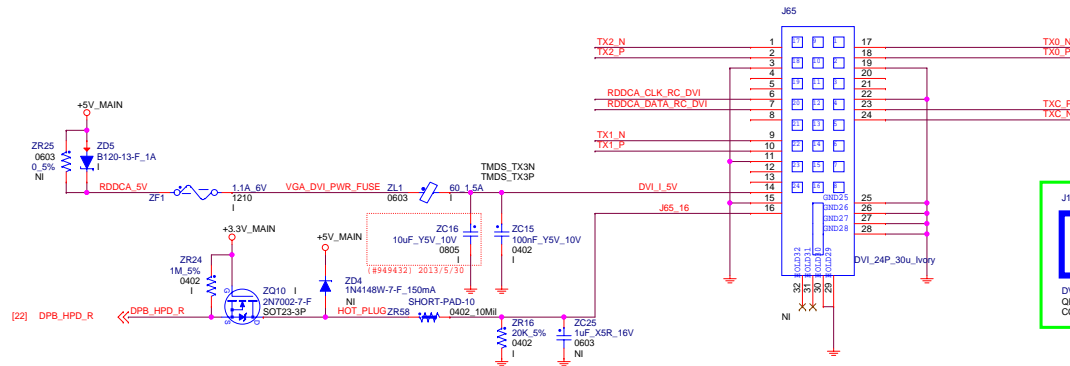


HP Restricted Secret.

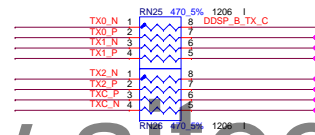
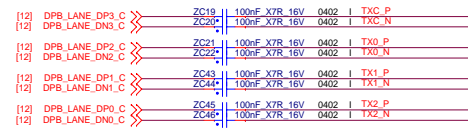
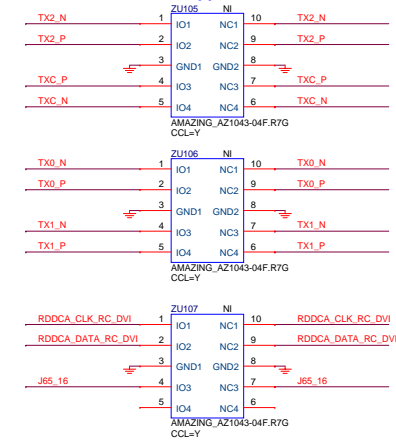
 <b>Hon Hai Precision Industry Co. Ltd.</b>	
<b>Foxconn NEW PCEBG DTSa</b> 2F, No.3-2, Chungshan Rd., Tu-cheng City, Taipei Hsien, Taiwan, R.O.C	
Phone: 886-2-7705-7999 Fax: 886-2-7705-7901	
<b>Title</b>	<b>PCIEx4+PCIEx1</b>
<b>Size</b>	<b>Document Number</b>
<b>Custom:</b>	<b>Skylake_Atayal</b>
<b>Free Modified: Thursday, August 06, 2016</b>	
16:17:09 /UTC+GMT / Sheet 42 of 7	



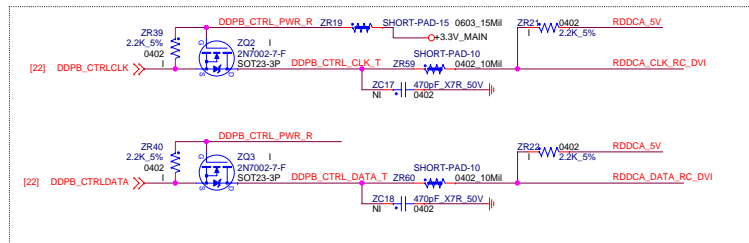
## DVI-D CONNECTOR



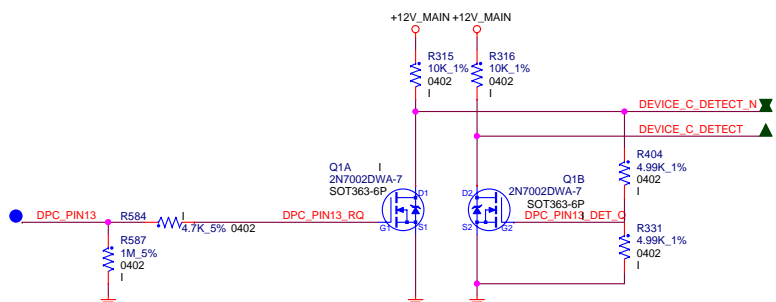
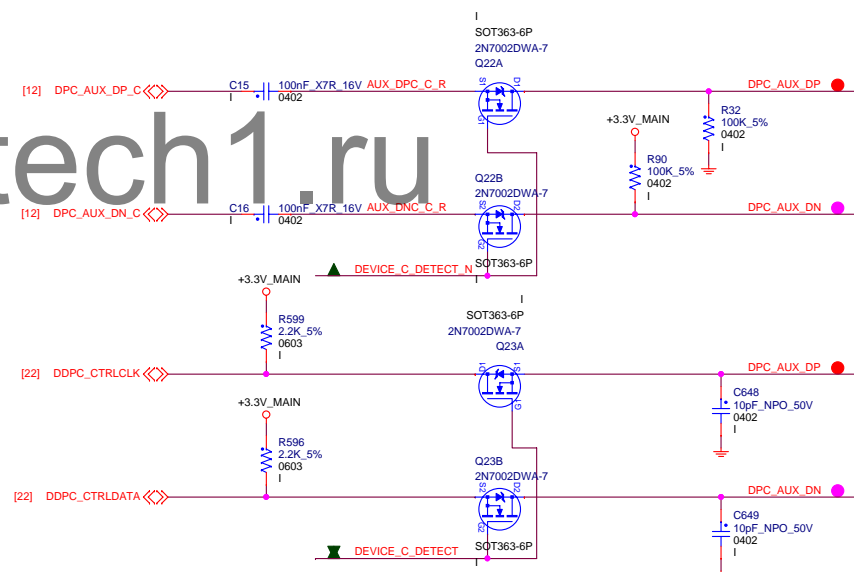
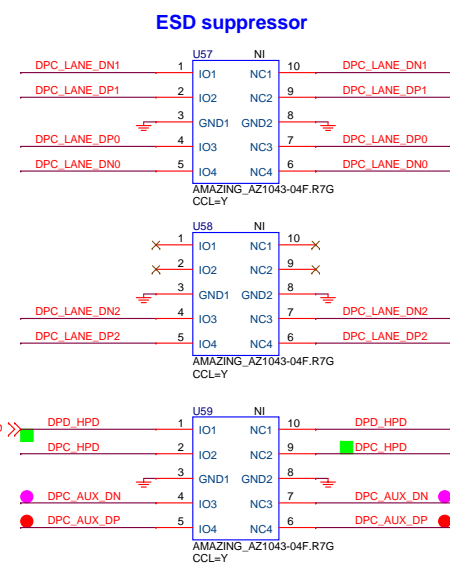
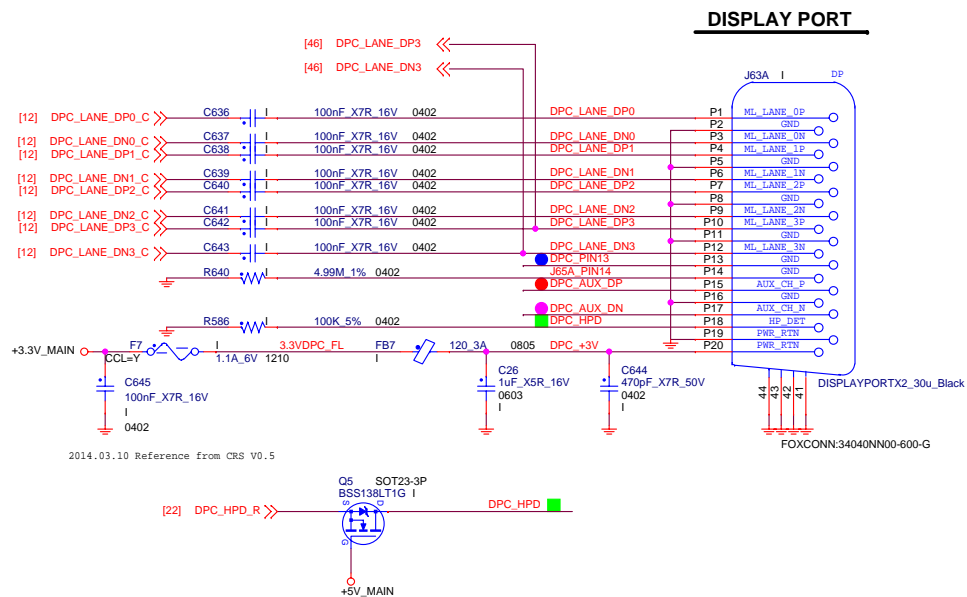
## ESD suppressor



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PIN13		FUNCTION
DP	DONGLE	
L	X	DEVICE_C_DETECT
X	H	DEVICE_C_DETECT_N

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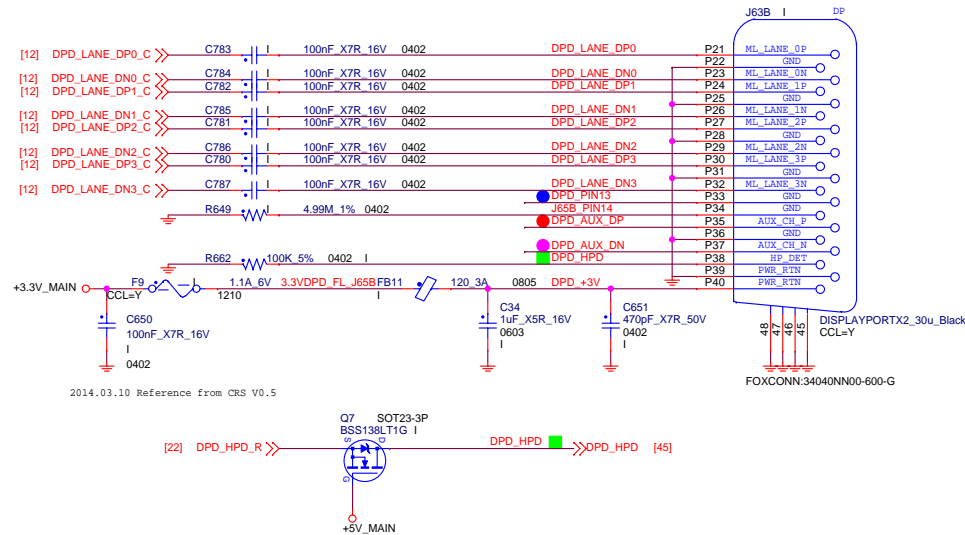
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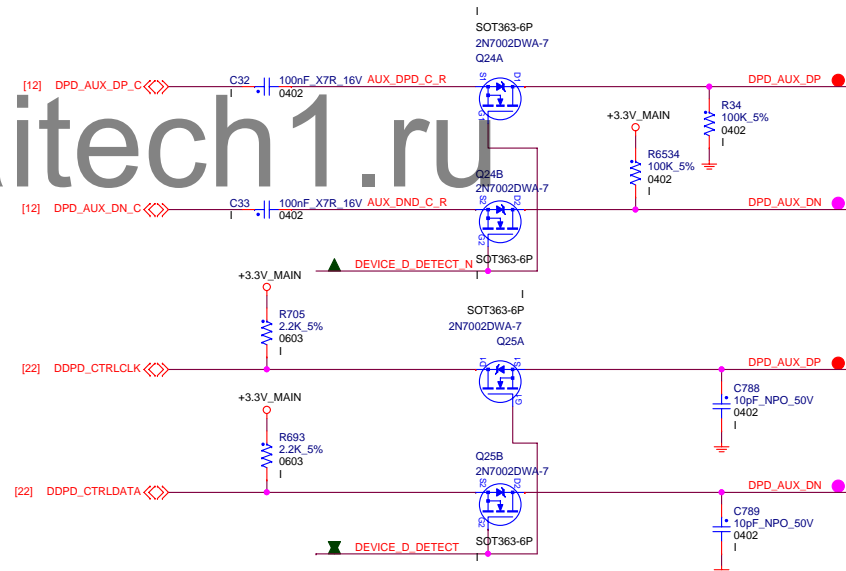
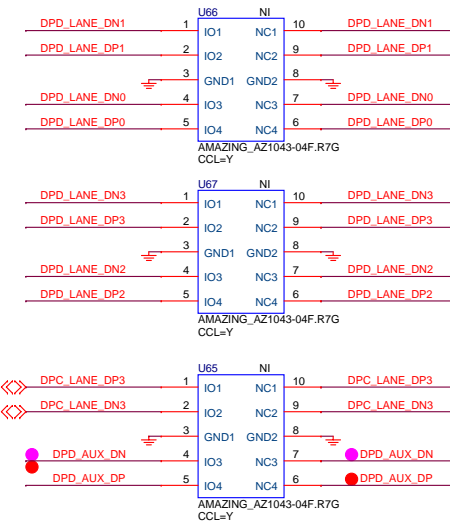
Title	DUAL DISPLAY PORT 1
-------	---------------------

Size Custom	Document Number Skylake_Atayal	Rev 3
Page Modified: Thursday, August 06, 2015		16:17:39 (UTC/GMT) Sheet 45 of 76

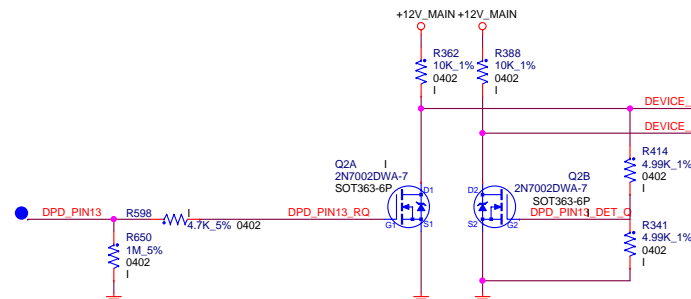
## DISPLAY PORT



ESD suppressor



PIN13		FUNCTION
DP	DONGLE	
L	X	DEVICE_D_DETECT
X	H	DEVICE_D_DETECT_N




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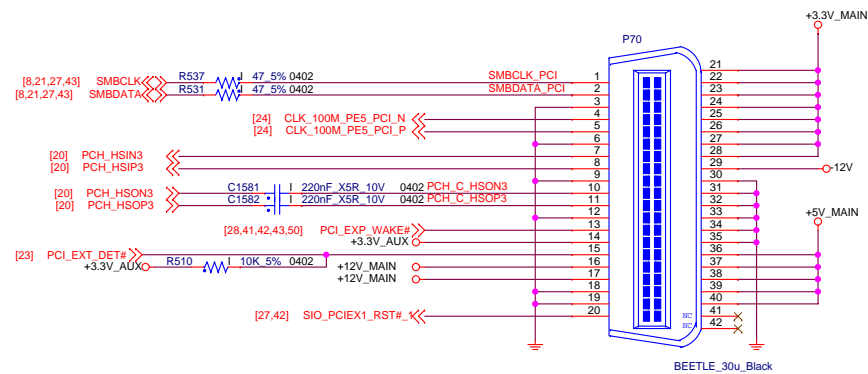
Tu-cheng City, Taipei Hsien, Taiwan, R.O	
Title	DUAL DISPLAY PORT 2

Size Custom	Document Number Skylake_Atayal	Re 3
Page Modified: Thursday, August 06, 2015		16:17:39 (UTC/GMT) Sheet 46 of 76



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<b>Title</b> <b>COM PORT HEADER</b>			
<b>Size</b> Custom	<b>Document Number</b> Skylake_Alayal		<b>Rev</b> B
<b>Page Modified:</b> Thursday, August 06, 2015		<b>16:17:58 (UTC+08C)</b>	<b>Sheet 47 of 76</b>



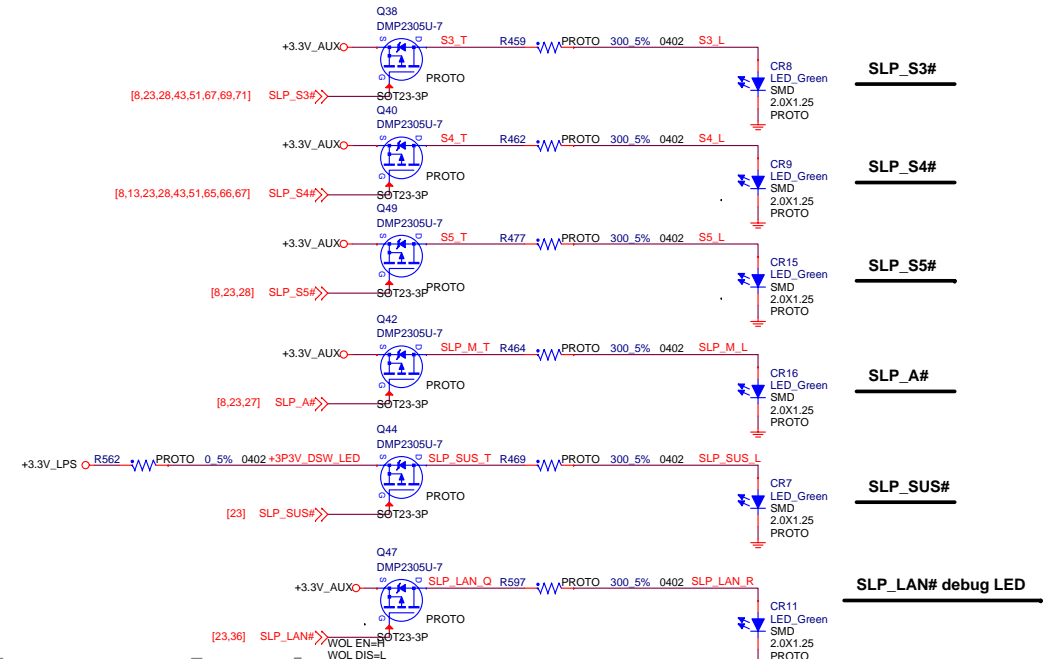
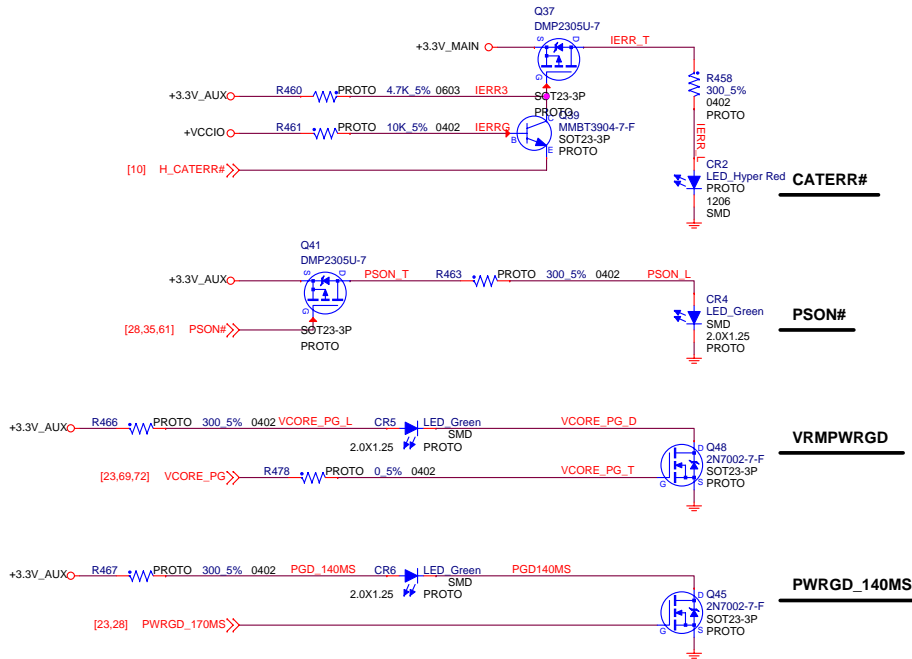


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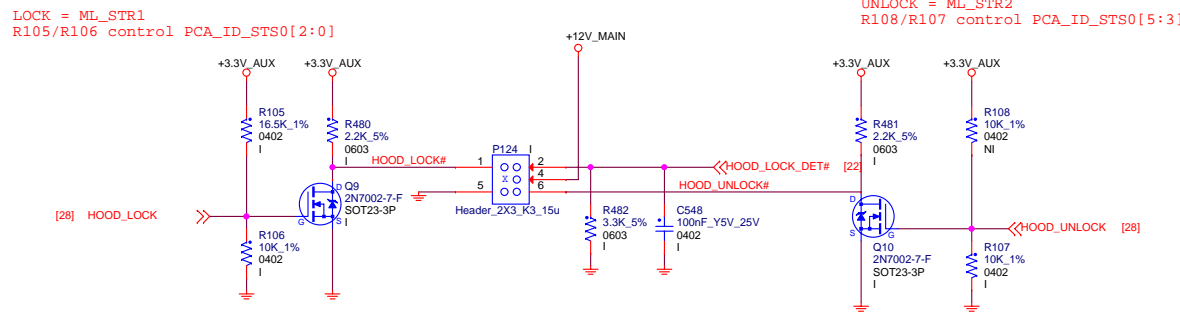
<b>FOXCONN</b>		Hon Hai Precision Industry Co. Ltd.	
<b>Foxconn NEW PCEBG DTSA</b>			
2F, No.3-2, Chungshan Rd., Tu-cheng City, Taipei Hsien, Taiwan, R.O.C		Phone: 886-2-7705-7999 Fax: 886-2-7705-7901	
Title <b>SCSI PCI EXTENDER</b>			
Size Custom	Document Number Skylake_Ataya1		Rev <b>B</b>
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## PCA LEDs

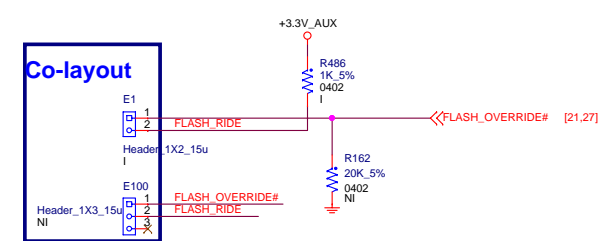


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## HOOD LOCK CIRCUIT

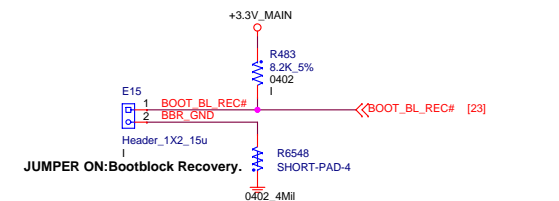


## FLASH OVERRIDE



## BOOTBLOCK RECOVERY

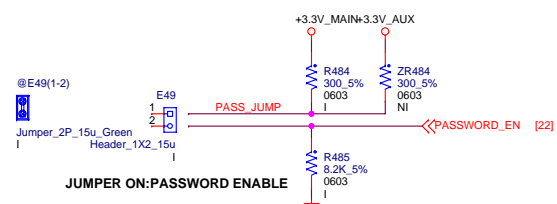
E15: SPI ROM bootblock recovery header



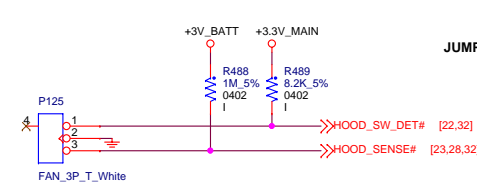
## PCA\_ID Resistor values

PCA Assignments	PCA_ID	ML_STR2 pin	ML_STR1 pin
SPITFIRE	0	NI	10K
SCORPION/BUNUN	1	NI	10K
TOLEDO	2	NI	10K
Atayal	3	NI	10K
	4	NI	10K
	5	NI	10K
	6	NI	10K
	7	NI	10K

## PASSWORD JUMPER



## HOOD SENSE CIRCUIT



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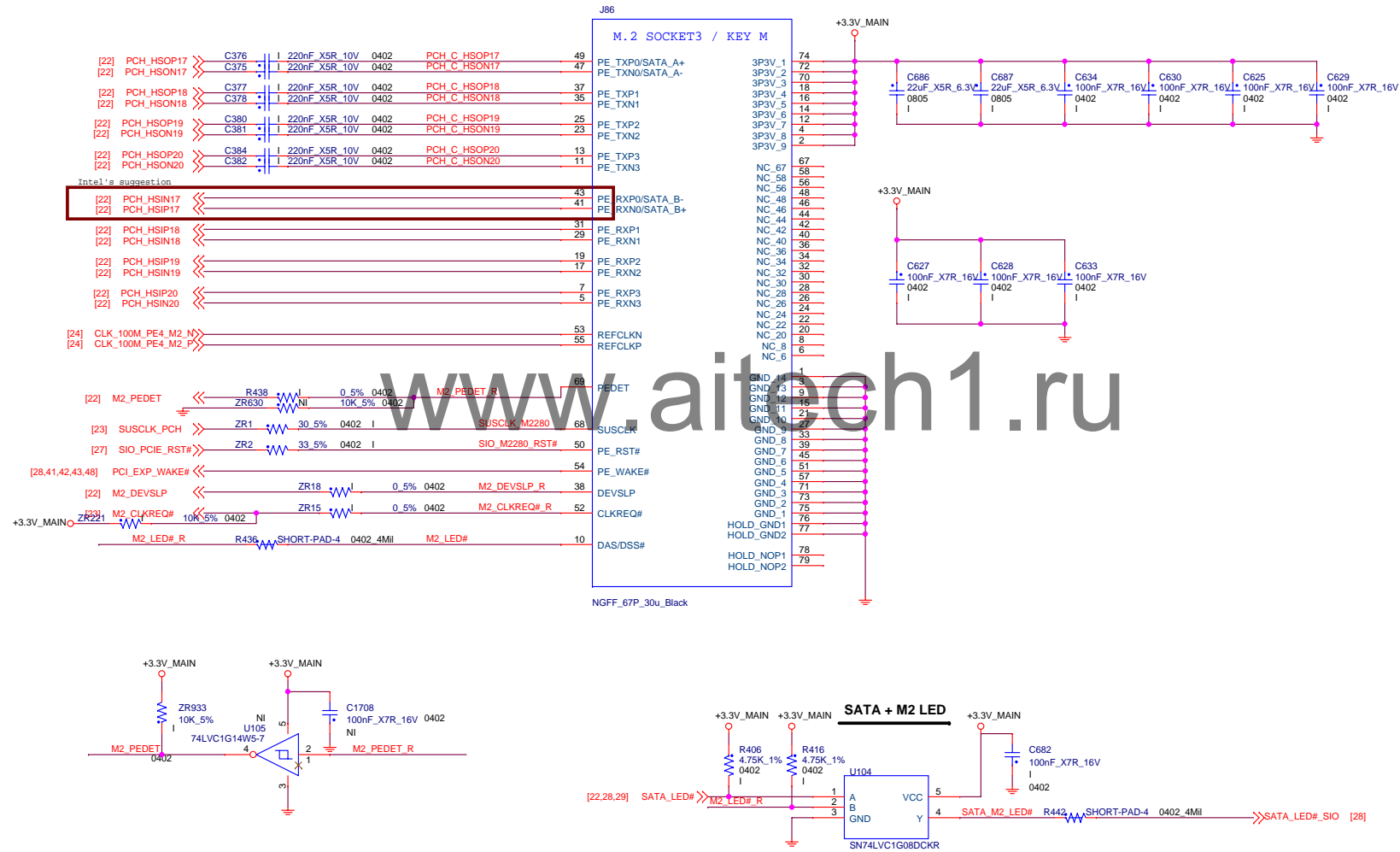
2F, No.3-2, Chungshan Rd., Tu-cheng City, Taipei Hsien, Taiwan, R.O.C. Phone: 886-2-7705-7999 Fax: 886-2-7705-7901

**LEDs/ HOOD LOCK\_SENSE**

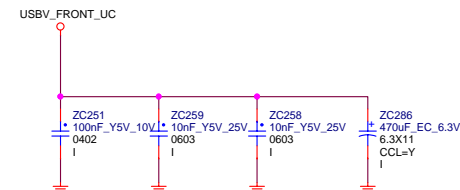
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## M2. 22110 - STORAGE



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State \ bit	CTL1 SLP_S3#	CTL2 SLP_S4#	CTL3 GPIO 41	ILIM_SEL GPIO 41	Mode	ILIM
S0	1	1	1	1	CDP	ILIM = 2510mA
S0	1	1	0	0	SDP	ILIM = 1525mA
S3	0	1	1	1	DCP_AUTO	ILIM = 2510mA
S3	0	1	0	0	SDP	ILIM = 1525mA
S4/S5	0	0	1	1	DCP	ILIM = 2510mA
S4/S5	0	0	0	0	TURN OFF SWITCH	ILIM = 1525mA

10-Cheng City, Taipei Dist., Taiwan, R.O.C.				Fax: 886-2-77057901	
Title <b>USB Charger</b>					
Size Custom	Document Number Skylake_Atayal				Rev <b>B</b>
Page Modified: Thursday, August 06, 2015		16:17:00 (UTC/GMT)		Sheet 51 of 76	

For PCIe16 and DMI signal

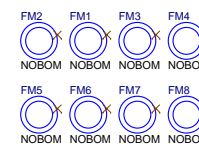
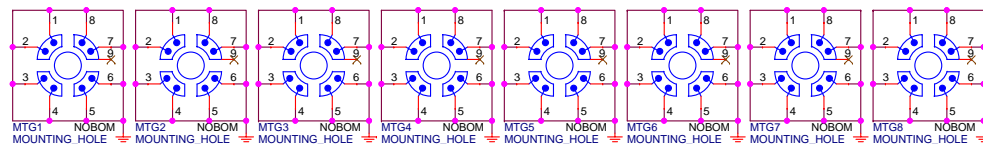
## EMI CAP

For M\_AB\_RESET\_N signal (Over moat)

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Title		Features 2	
Size	Document Number	Rev	
Custom	Skylake_Atayal	B	
Page Modified: Thursday, August 06, 2015		16:17:36 (UTC+GMT) Sheet 52 of 76	



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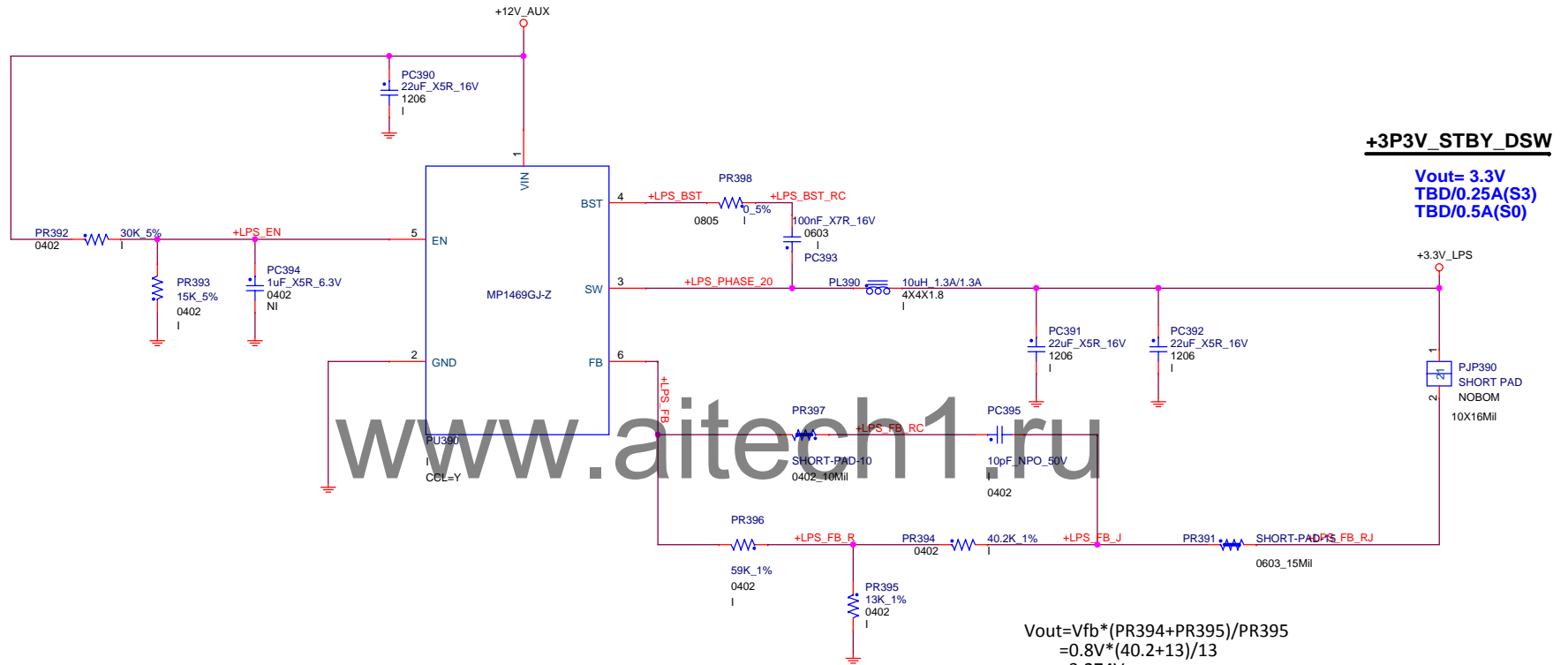
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## +3P3V LPS



$$V_{out} = V_{fb} * (PR394 + PR395) / PR395$$

$$= 0.8V * (40.2 + 13) / 13$$

$$= 3.274V$$

Current Limit: Type Value = 3A

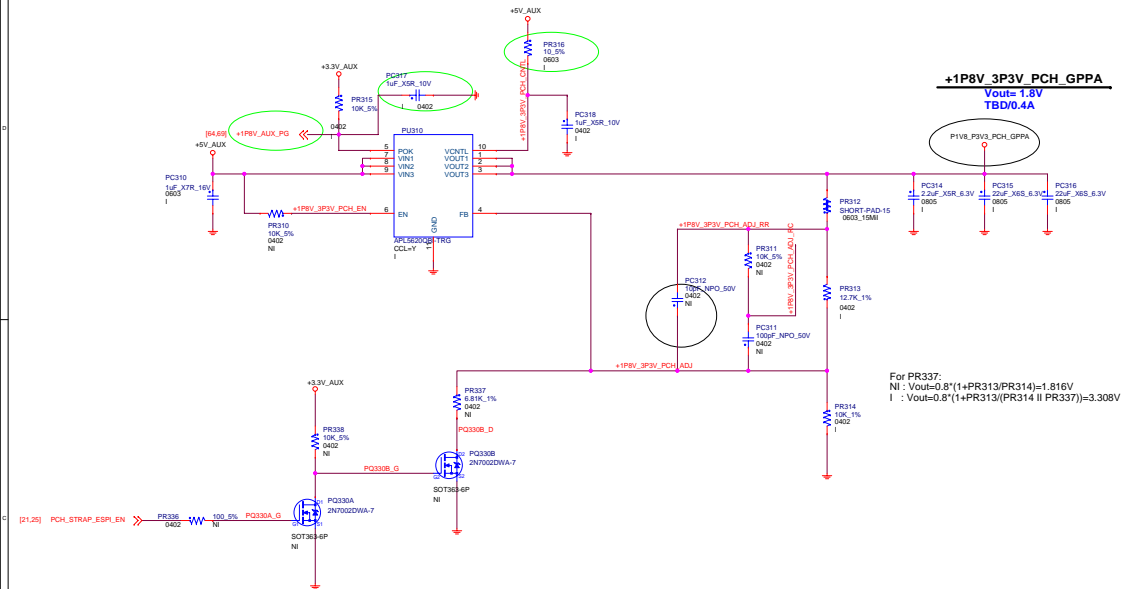
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+1P8V\_3P3V\_PCH




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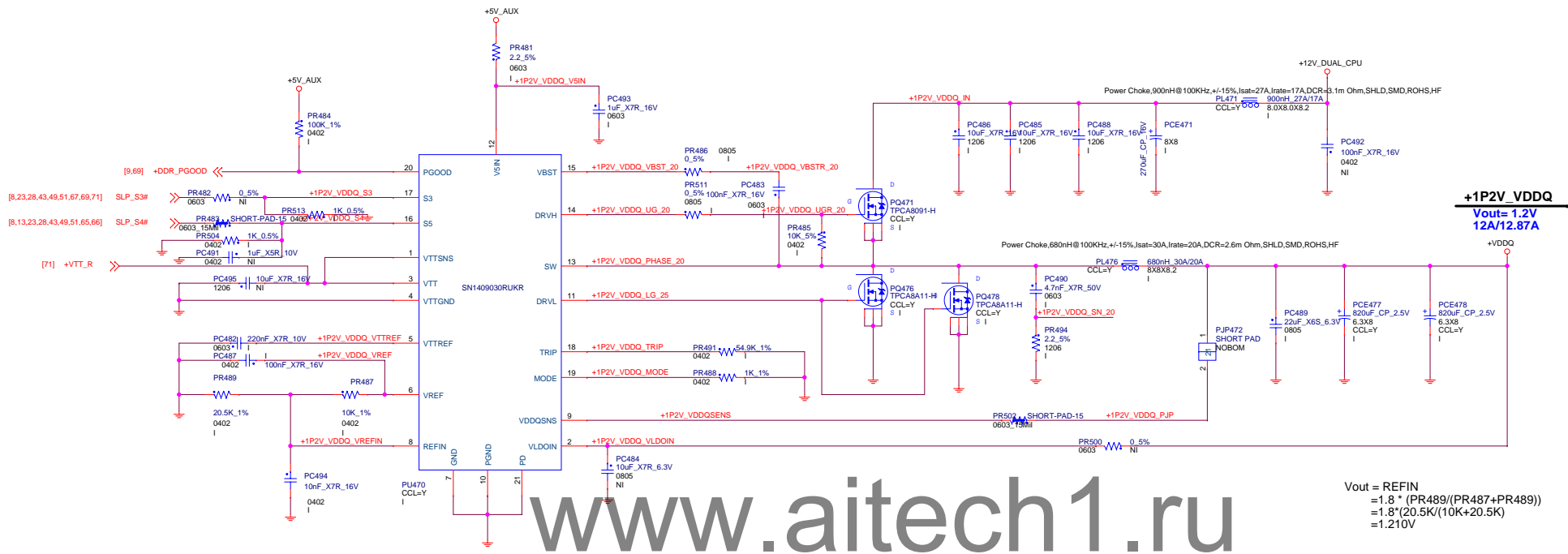




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<b>Title</b> +1.2V_SFCRO			
<b>Size</b> Custom	<b>Document Number</b> Skyline_Atupal		<b>Rev</b> B
<b>Page Modification</b> Thursday, August 08, 2013		16:17:38 (UTC+08T)	Sheet 65 of 78



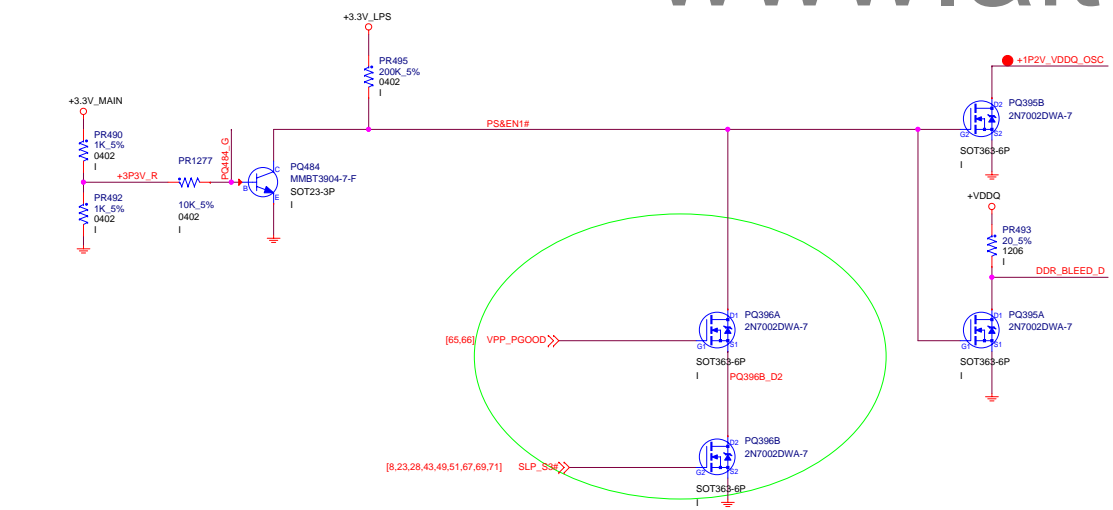
# **+1P2V\_VDDQ**




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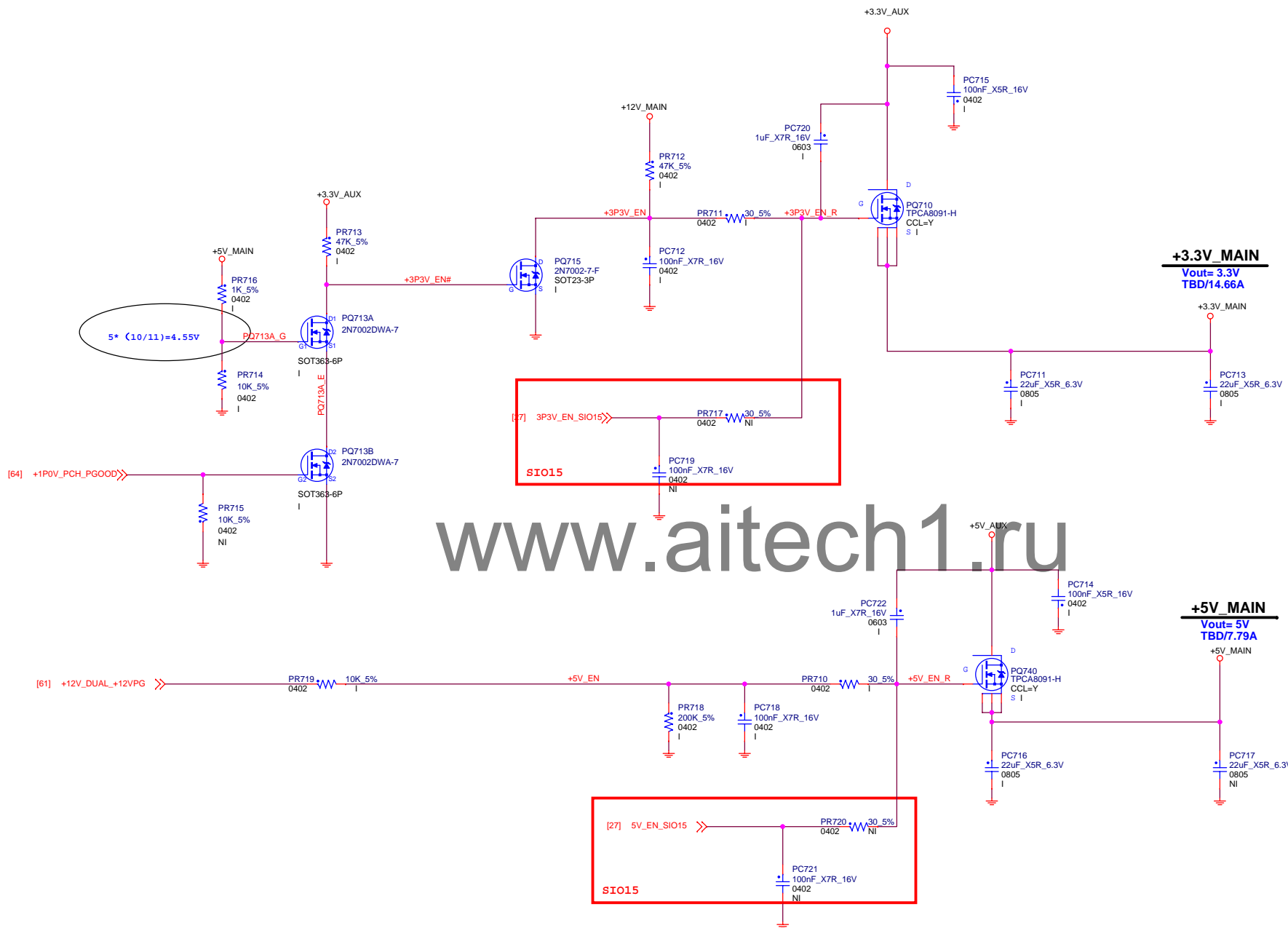
Vout = REF1N  
 = 1.8 \* (PR489/(PR487+PR489))  
 = 1.8 \* (20.5K/(10K+20.5K))  
 = 1.210V

## **+1P2V\_VDDQ BLEED OFF**




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Title  +1P2V_VDDQ			
Size Custom	Document Number <b>Skylake_Atalay</b>		Rev <b>B</b>
Page Modified: Thursday, August 06, 2015		14:17:49 (UTC+08:00)	Sheet 67 of 76

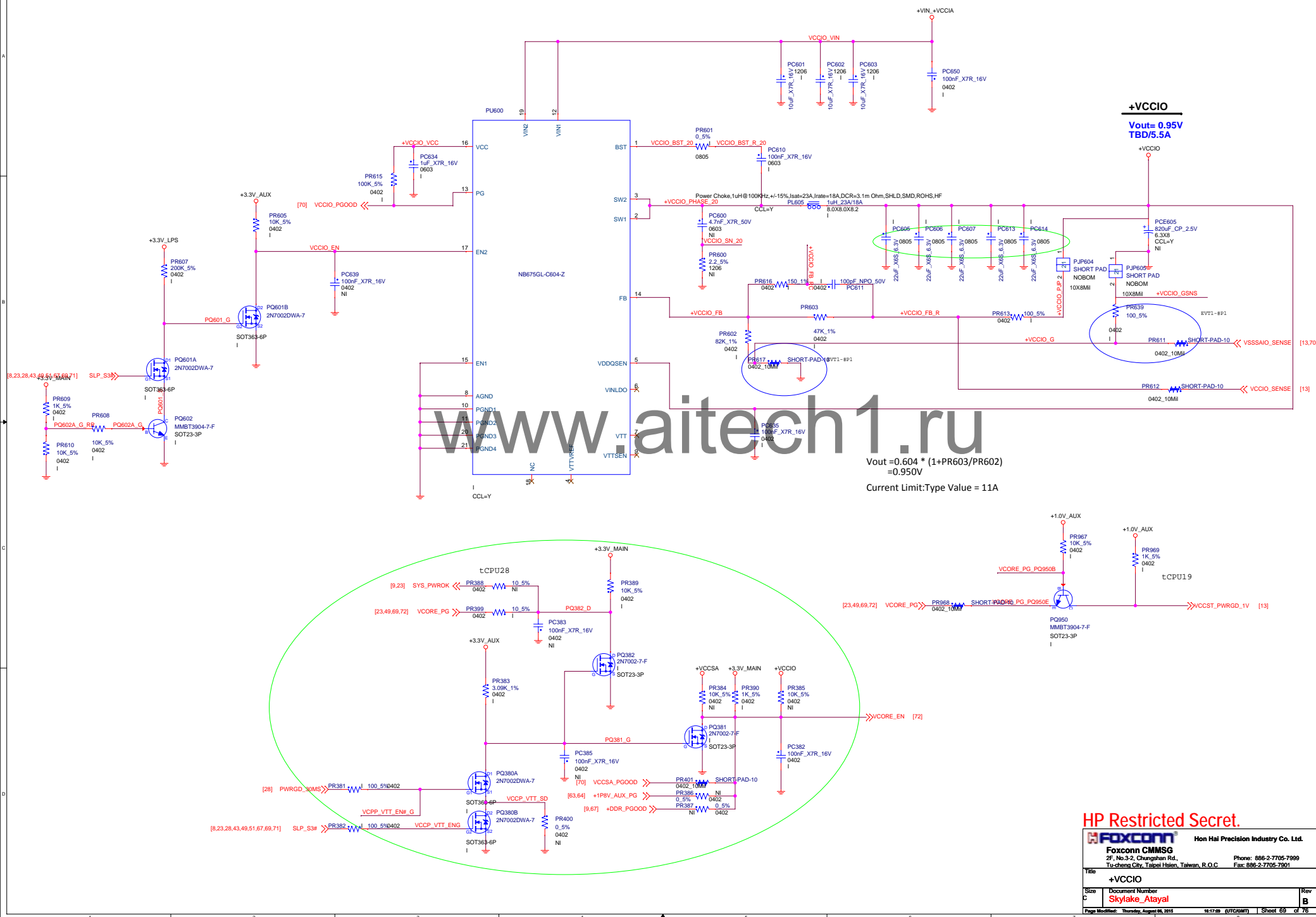


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Title <b>+3.3V_MAIN &amp; +5V_MAIN</b>			
Size Custom	Document Number <b>Skylake_Atayal</b>	Rev B	
Page Modified: Thursday, August 06, 2015		16:17:58 (UTC/GMT)	Sheet 68 of 76



Note: net-name:Convertor 3



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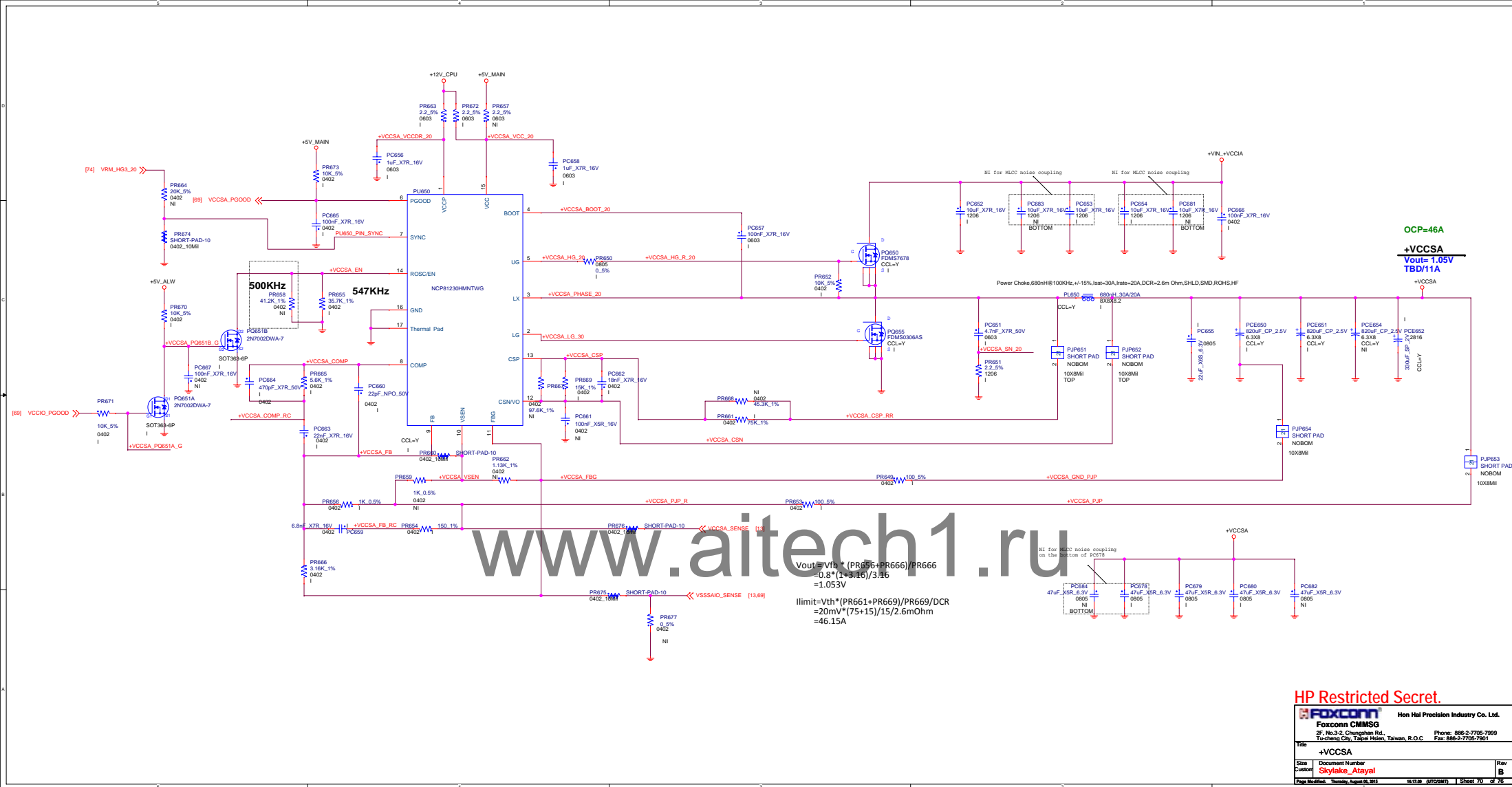
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Tu-cheng City, Taipei Hsien, Taiwan, R.O.C  
Phone: 886-2-7705-7999  
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Title	+VCCIO
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Size	Document Number
C	Skylake_Atayal

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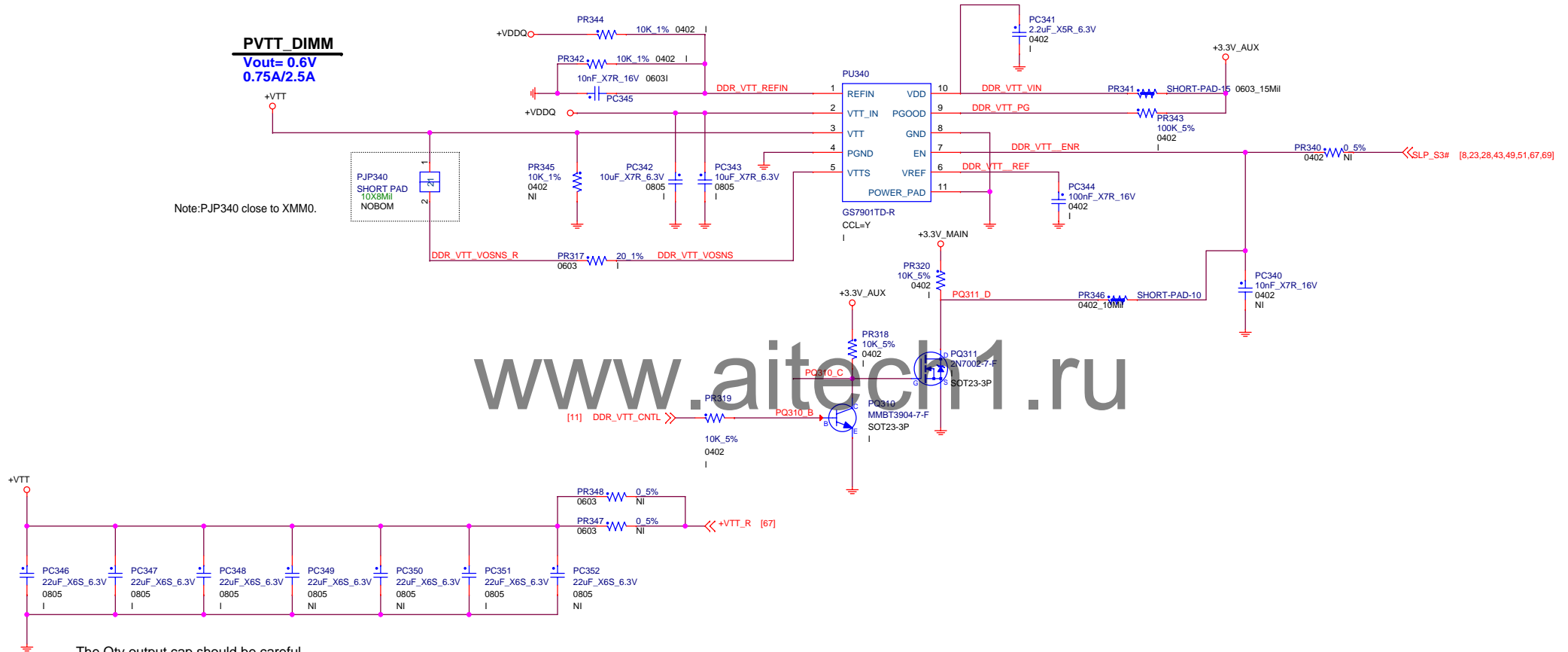
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<b>Title</b> +VCCSA			
<b>Size</b> Custom	<b>Document Number</b> Skylake_Atayai		
Page Modified: Thursday, August 05, 2015		14:42:09 67C0287F	
		Sheet 70 of 70	

# DDR\_VTT


**PVTT\_DIMM**  
Vout= 0.6V  
0.75A/2.5A

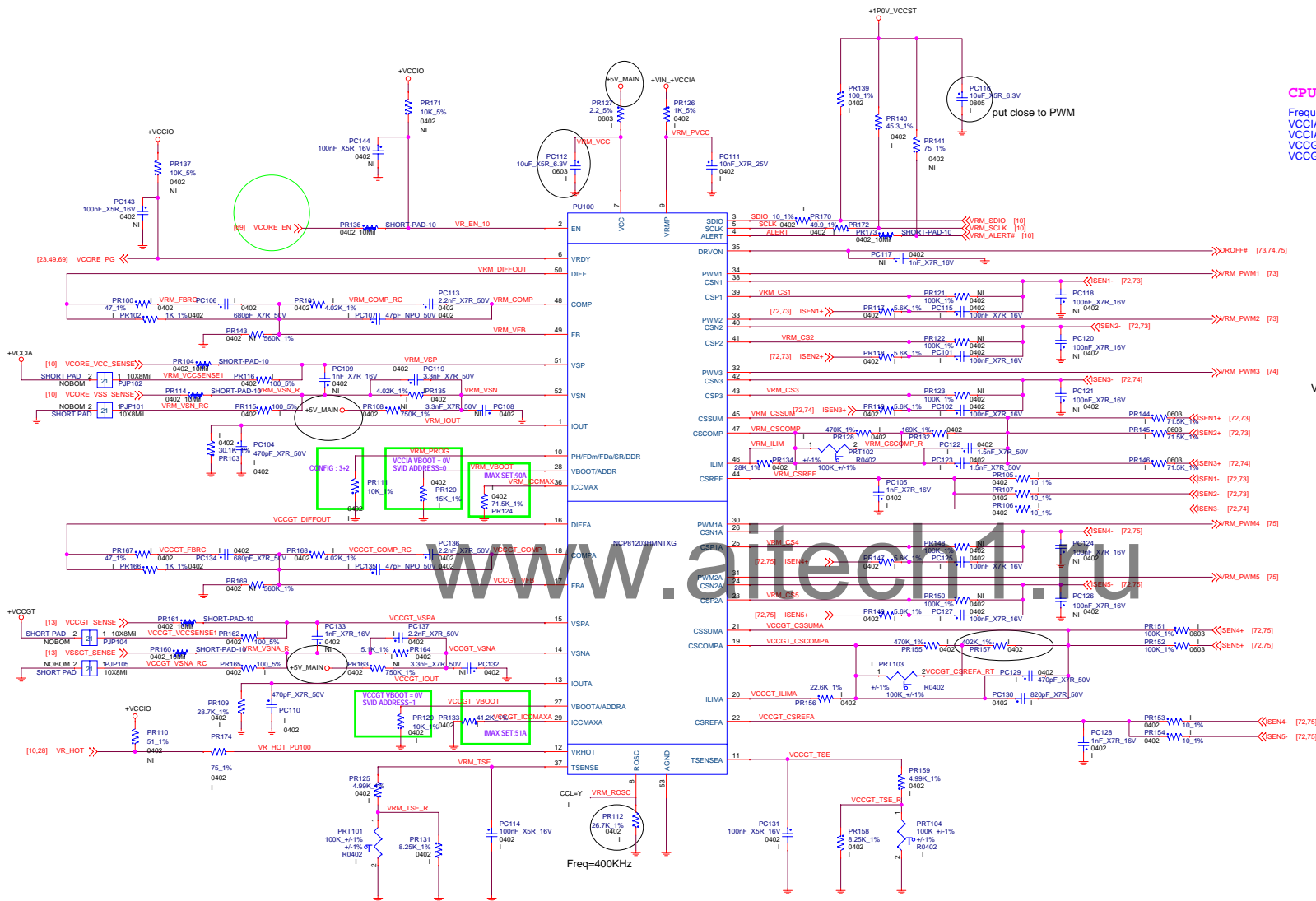
Note:PJP340 close to XMM0.



The Qty output cap should be careful  
INTEL: the latest modeling shows step load size 6-9x higher than it's shown in PDG  
1.0 for Aztec City CRB

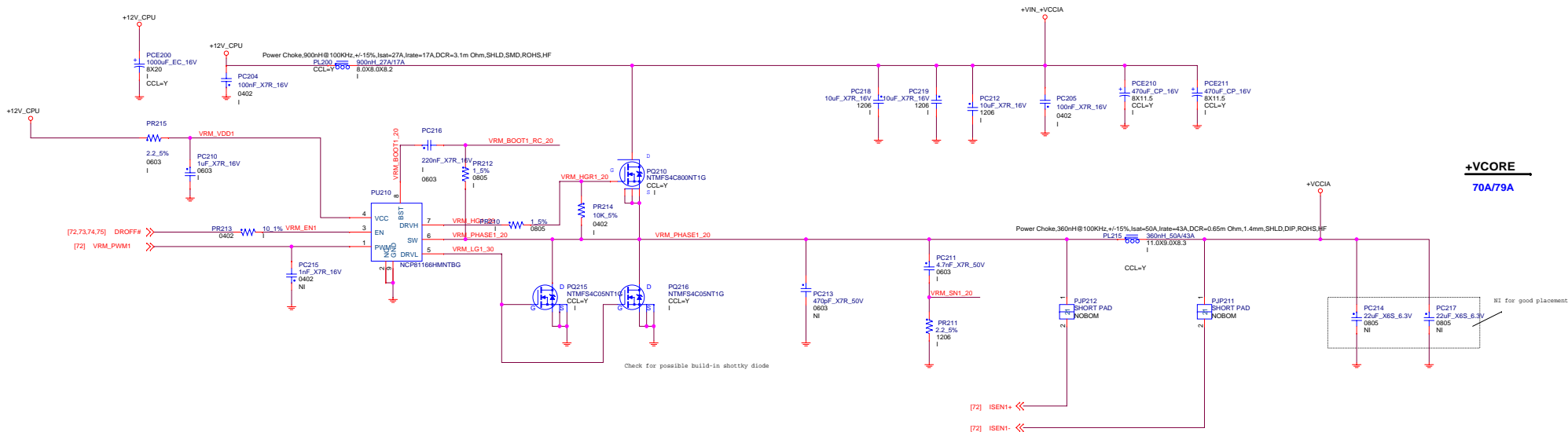
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Title <b>+VTT</b>			
Size Custom	Document Number <b>Skylake_Ataya</b>		Rev <b>B</b>
Page Modified: Thursday, August 06, 2015		16:17:59 (UTC/GMT)	Sheet 71 of 76

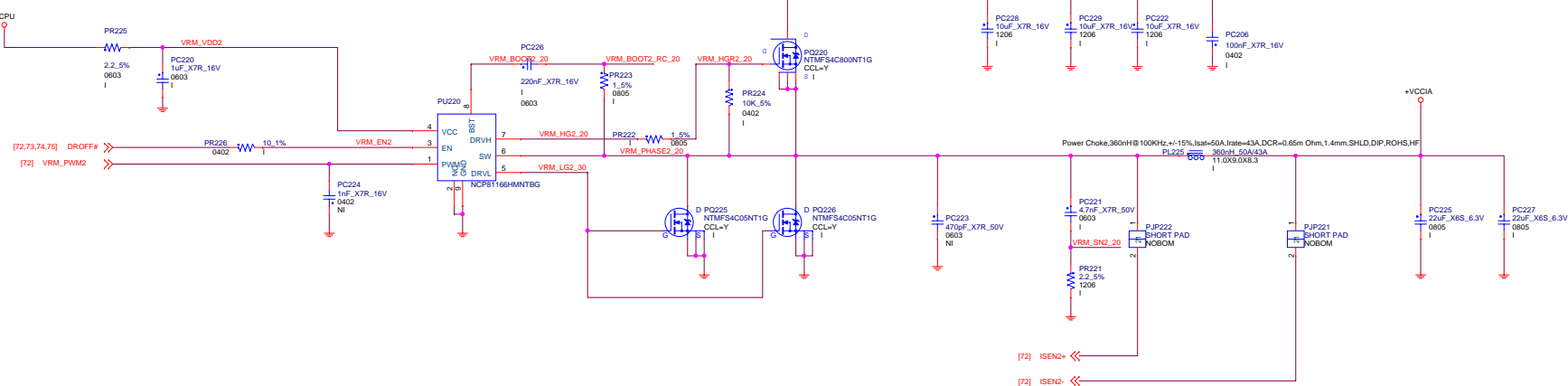


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# VCORE PHASE1~2



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ITEM	DATE	PAGE	ID	CHANGE DESCRIPTION
For EVT2				
#P1	2014/8/27	69	3	VCCIO sense loops resistance modify
For DVT				
#P2	2014/10/6	63	84	Ventl of PIV8_P3V3_PCH_GPPA be dropped to 3.5V, change PR316 to 10_5% 0603.
#P3	2014/10/7	63	84	Vout of PIV8_P3V3_PCH_GPPA is 2.8V, change PR337 to 6.81K_1% 0402.
#P4	2014/10/6	71	84	Vin of VTT be dropped to 2.5V, Change PR341 to 0_5%
#P5	2014/10/6	71	84	VTT no power (slp_s3# be pulled low) add a PR320 10K_5%.
#P6	2014/10/6	61	84	+12V_Dual no power,due to +12V_LPS_ON# pull low connect +12V_LPS_ON# to LPS_ON#
#P7	2014/10/17	69	84	Add PR967,PR968,PR969 for isolation circuit of VCORE_PG and VCCST_PWRGD_IV.
#P8	2014/10/21	64	85	+1.0V_AUX GM/PM test fail,modified as below: Change PC526 from I to NI; Change PC525 from 2.2nF_X7R_50V to 1nF_X7R_50V; Change PC524 from 33nF_X7R_16V to 6.8nF_X7R_16V; Change PR522 from 24_1% to 34_1%; Change PR527 from 4.02K_1% to 3.92K_1%.
#P9	2014/10/21	70	86	VCCSA GM/PM and efficiency tes fail, modified as below: Change PR658 from I to NI; Change PR655 from NI to I; Change PC659 from 33nF_X7R_16V to 6.8nF_X7R_16V; Change PR654 from 24_1% to 150_1%.
#P10	2014/10/21	66	87	+VPP GM/PM fail,modified as below: Change PC636 from 220pF_X7R_50V to 47pF_NPO_50V
#P11	2014/10/21	73, 74, 75	88	EVT2 change CPU VR MOSFET from Dr.MOS to discrete MOS
#P12	2014/10/21	68	SIO01090142	VCCIO GM/PM and efficienvy test fail, modified as below: Change PL605 from 2.2uH to 1uH; Change PR616 from 499_1% to 150_1%; Change PC611 from 220pF_X7R_50V to 100pF_NPO_50V
#P13	2014/12/1	68	SIO01090142	Change VTT enable from S3# to DDR_VTT_CNTL. PR340 was change from I to NI PR346 was change from NI to I PR320 was change from NI to I PQ311 was change from NI to I PR319 was change from NI to I PQ310 was change from NI to I PR318 was change from NI to I
	2015/1/9	67	SI01110021	Fix VDDQ DDR4 VRTT fail issue PR489 was changed from 20k to 20.5k PL476 was changed from 1uH to 0.68uH
		70	SI01110038	Fix VCCSA VRTT fail issue PR665 was changed from 4.99K to 5.6k Ohm PR655 was changed from 249k to 35.7k Ohm PL650 was changed from 1uH to 0.68uH PR669 was changed from 21.5k to 15k Ohm PC660 was changed from 33pF to 22pF PC681 was removed from schematic PC682 was set from I to NI PR661 was changed from 78k to 75k Ohm PCE652 was added. 330uF low profile(1.5 mm high) sp cap in CPU cavity

	2015/1/9	67	SI01117191	VTT solution change for meet tCPU18 requirement. PU340 was changed from TPS51200 to GS7901TD-R PC340 was set from I to NI
	2015/1/9	72	SI0115825	VCCIA Iccmax update from 79 to 90 A PR134 was changed from 23.7k to 28k Ohm PR124 was changed from 63.4k to 71.5k Ohm PR103 was changed from 28.7k to 30.1k Ohm
	2015/1/16	72	SI01096009	PROC_HOT impedance correction, #543611 PR174 was added regarding to intel spec 543611. 75 ohm
	2015/1/25	72	SI01110663	P3 cable leakage solution Change connection of PR774 from +12V_MAIN to +12V_CPU
	2015/1/23	62	SI01110127	+5V abnormal operation PR944 was set from I to NI
	2015/1/29	62	SI01094554	Fix for USB short and shutdown issue, increase OCP to 55A of +5V_AUX Change PR918 to 19.1K_1% Change PR919 to 10.2K_1%
	2015/2/2	60	SI01116943	Fix for fullfill main and second source BOM Change PR397 to 0 Ohm and set to I Change PC395 to 10pF and set to I Change PC349, PC350, PC352 from I to NI
	2015/2/2	72	SI01115825	NCP81203 change Rev BC to CA PR128 was changed from 240k to 470k PR120 was changed from 10K to 15K PR155 was changed from 280k to 470k PC129 was changed from 560pF to 470pF
PVT1				
	2015/3/13	67	SI01128595	Reserve PC491 1uF_X5R_10V 0402 for VPP and VDDQ sequence
	2015/3/13	73	SI01126992	Change PR388 from I to NI for tCPU28
				Change PR104,PR114,PR136,PR160,PR161,PR346,PR397,PR401,PR512,PR530,PR611,PR612,PR617, PR660,PR674,PR675,PR676,PR785,PR906,PR912,PR916,PR936,PR968,PR1315 from 0_5% 0402 to SHORT-PAD-10 0402_10Mil
	2015/3/31	SI01135524		Change PR173, from 0_1% 0402 to SHORT-PAD-10 0402_10Mil
				Change PR314,PR341,PR391,PR483,PR502,PR904,PR905,PR932 from 0_5% 0603 to SHORT-PAD-15 0603_15Mil
				Change PR630,from 0_1% 0603 to SHORT-PAD-15 0603_15Mil for design improvement.
	2015/3/31	SI01135420		Change PC215,PC224,PC234, PC277, PC298 from I to NI for PWM non-delay
	2015/4/22	63	SI01144512	Change PQ330,PR338,PR336 from I to NI
		70, 73, 74, 75	SI01130457	Change PQ650,PQ210,PQ220,PQ230,PQ270,PQ290 from NTMFS4C800NTIG to FDMS7678 for BOM controll
	2015/4/22			Change PQ655,PQ215,PQ216,PQ225,PQ226,PQ235,PQ236,PQ275,PQ276,PQ295,PQ296 from NTMFS4C03NTIG to FDMS0302S for BOM controll
	2015/5/4	62, 64, 67, 70, 73, 74, 75	SI01154329	For BOM controll Change PQ210,PQ220,PQ230,PQ270,PQ290 back from FDMS7678 to NTMFS4C800NTIG Change PQ215,PQ216,PQ225,PQ226,PQ235,PQ236,PQ275,PQ276,PQ295,PQ296 from FDMS0302S to NTMFS4C05NTIG Change PQ655 from FDMS0302S to FDMS0306AS ChangePQ710,PQ740,PQ510,PQ930,PQ940,PQ471 from NTMFS4C800NTIG to TPCA8091-H Change PQ935,PQ936,PQ945,PQ946,PQ515,PQ476,PQ478 from NTMFS4C760NTIG to TPCA8A11-H

					PVT2
	2015/6/3	62	SI01169422		Reserve +3.3V_AUX Bleed off Circuit for HP request
	2015/6/10	70, 74, 75	SI01168630		Reserve PC237,PC241,PC681,PC683,PC284,PC282,PC295,PC288,PC289,PC290,PC242,PC243,PC244 for MLCC noise coupling Delete PCE653 for noise coupling placement
	2015/6/17	62	SI01169422		Change +3.3V_AUX Bleed off Circuit from NI to I for HP request
MVB					
	2015/7/28	73	SI01168630		PCE210, PCE211 were changed from 270uF to 470uF 16V Oscon by HP request.

HP Restricted Secret.

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